©1997 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

This copyright notice is taken from the IEEE PSPB Operations Manual, section 8.1.10 entitled "Electronic Information Dissemination". At the time of this notice, this section is posted at

http://www.ieee.org/portal/index.jsp?pageID=corp_level1&path=about/documentation/copyright&file=policies.xml&xsl=generic.xsl

Subthreshold Analysis of an MOS Analog Switch

Saeed Aghtar, *Student Member, IEEE,* J. W. Haslett, *Senior Member, IEEE,*
and F. N. Trofimenkoff, *Senior Member, IEEE,*

Abstract— **Charge injection error in the presence of subthreshold effects has been analyzed. It is confirmed that the subthreshold effect is significant at low voltage falling rates. A simplified model is derived using an appropriate approximation. Predictions are compared to the results of a SPICE simulation, a nonquasi-static (NQS) model simulation and experimental results. Excellent agreement between the modified and NQS model and recently published experimental results was obtained. This analytical model is computationally efficient compared to the SPICE and NQS models and provides physical insight into the switching errors.**

I. Introduction

The charge injection error in switches is one of the factors limiting the accuracy of high-speed circuits. This effect reduces the performance and maximum clock frequency of the circuits in applications such as sample-and-hold stages, A/D converters, switched-capacitor and switched-current filters. The accuracy of instrumentation circuits also suffers from this error.

Attempts have been made to model switch charge injection error using the simplified circuit of Fig. 1.

A qualitative observation regarding a simplified case was made by MacQuigg [1]. Sheu and Hu proposed an analytical model assuming infinite source capacitance, C_S [2]. Equations for the general case were derived and solved numerically by J. H. Shieh *et al.* [3], [4]. This model was also validated with experimental evidence and its limitations were delineated by G. Wegmann *et al.* [5]. All of these results are based on an equivalent lumped model for the transistor. Different charge conserving nonquasi-static (NQS) models have also been proposed for the transient analysis of a transistor and used for the charge injection error calculation [6], [7]. Although these models guarantee node charge conservation [7] and the results are found to be in very good agreement with experimental results, they are very complicated and computationally inefficient.

All the analyzes have shown that a slow switching rate and small transistor size can help reduce the charge injection error. In some instrumentation applications speed is not critical whereas on-resistance plays an important role in the accuracy of the circuit. In these applications speed can be traded for accuracy by lowering the switching rate to decrease the charge injection error. The transistor size can be maintained fairly large for a low on-resistance. At low gate voltage falling rates,

Manuscript received April 22, 1996. The review of this paper was arranged by Editor D. P. Verret. This work was supported by NSERC under Grants OGP0007776 and OGP0003382, and by the Canadian Microelectronics Corporation.

The authors are with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, Alberta T2N 1N4, Canada.

Publisher Item Identifier S 0018-9383(97)00311-0.

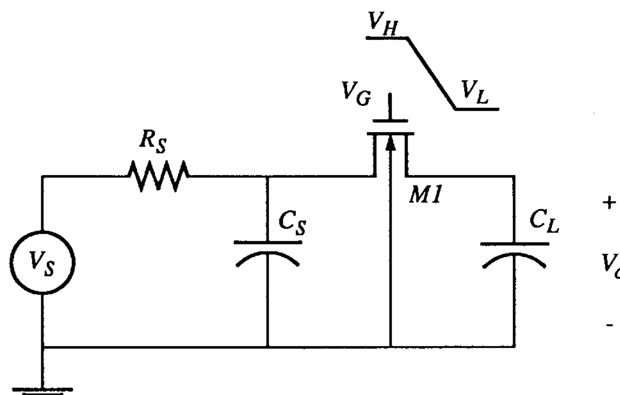


Fig. 1. Circuit for charge injection analysis.

as the error due to charge injection decreases and the transistor transient time from ON to OFF increases, the subthreshold effect becomes more important. The importance of this effect has recently been demonstrated experimentally [8]. This effect has not been analytically considered in any of the published results based on the lumped model.

To include the subthreshold effects, this paper modifies Sheu and Hu's model [2] by adding the subthreshold current and inversion layer charge variation effect in the weak inversion region. The variation of the gate–source capacitance above the threshold voltage is also taken into account. An approximation is used to find an analytical solution for the final charge injection error. The modifed model is simple, computationally efficient and provides physical insight into the switching errors in the weak inversion region.

Sheu and Hu's model is described in Section II. The modified model is explained in Section III. The analytical model for the final error is derived in Section IV. The dependence on process and electrical parameters is considered in Section V. Section VI is devoted to briefly explain a charge conserving nonquasi-static (NQS) model [7] which will be referred to as the NQS-model throughout this paper. The simulation results comparing the modified model with the NQS and SPICE models are presented in Section VII. The effect of source capacitance is discussed in Section VIII. A conclusion is given in Section IX.

II. Sheu and Hu's Model

This model was developed based on Fig. 1, assuming zero source resistance and capacitance so that $M1$ is connected directly to the voltage source V_S. The fraction of the channel charge that escapes to the substrate (charge pumping effect) is also neglected. It has been shown that in a practical case the charge pumping effect is insignificant in a short-channel transistor [5].

0018–9383/97$10.00 © 1997 IEEE

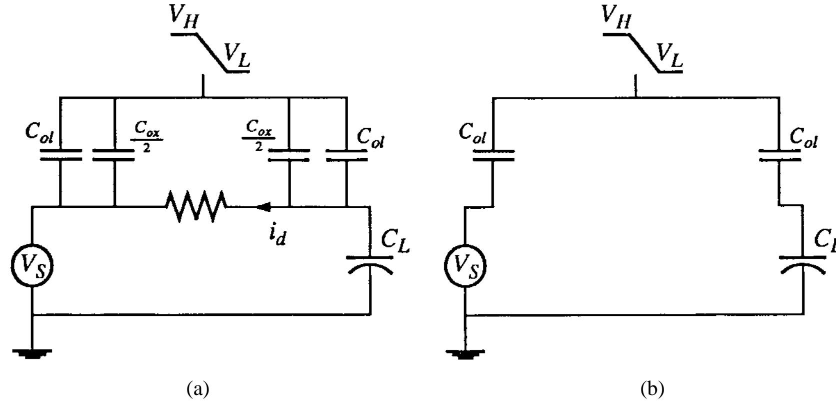


Fig. 2. Equivalent lumped model for the analog switch. (a) Transistor is ON. (b) Transistor is OFF.

Two phases of operation are considered during the turn-off transient. In the first phase, the transistor is ON ($V_G \geq V_S + V_T$, where V_T is the transistor threshold voltage), and the channel current i_d, contributes to the cancellation of the charges injected by the gate–oxide capacitance ($C_{\rm ox}$) and gate–overlap capacitance ($C_{\rm ol}$) [Fig. 2(a)]. In the second phase, the transistor is OFF ($V_G \leq V_S + V_T$) and the output error voltage is increasing only due to the overlap capacitance [Fig. 2(b)].

A ramp function is assumed for the gate voltage as shown in Fig. 3. In Phase 1

$$C_L \frac{dv_d}{dt} = -i_d - \left(C_{\rm ol} + \frac{C_{\rm ox}}{2}\right)U \tag{1}$$

where

$$i_d = \beta(V_{HT} - Ut)v_d. \tag{2}$$

In (2), v_d is the output error voltage, β is the transistor conductance coefficient ($\mu C'_{\rm ox}\frac{W}{L}$), U is the gate voltage falling rate and $V_{\rm HT}$ is defined as

$$V_{\rm HT} = V_H - V_S - V_T.$$

The solution to this differential equation is shown in (3), at the bottom of the page.

In the second phase, no current flows through the channel and the output error voltage is due to the charge injected by the overlap capacitance. Thus the overall error voltage at the end of this phase ($V_G = V_L$) is

$$v_{\rm df} = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{\rm ol} + C_{\rm ox}/2}{C_L}\right)\text{erf}\left(\sqrt{\frac{\beta}{2UC_L}}V_{\rm HT}\right) - \frac{C_{\rm ol}}{C_L}(V_S + V_T - V_L). \tag{4}$$

III. Modified Sheu and Hu's Model

The analysis in Section II shows that a smaller gate voltage falling rate and transistor size produce a lower output error voltage. However, lower on-resistance requires a larger transistor size. In high-accuracy applications where low on-resistance is essential, a slow gate voltage falling rate can decrease the error. When the charge injection error is decreased, second order effects which are not considered in Sheu and Hu's analysis play a significant role. In this section, the subthreshold current and weak inversion channel charges are added to the model described in the previous section.

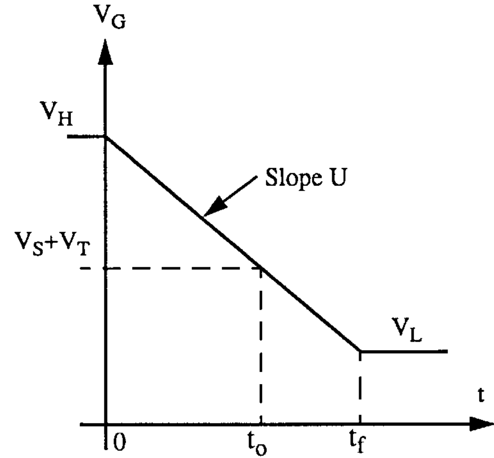


Fig. 3. Definition of the applied gate voltage.

A. The Subthreshold Current

The diffusion current in a MOS transistor is significant compared to the total drain current when the gate–source voltage is below the threshold voltage. When $V_{\rm GS} \ll V_T$, the drain current can be modeled accurately with an exponential function. In moderate inversion, where the gate–source voltage approaches the threshold voltage, both diffusion and drift current contribute significantly to the drain current. It is well known that a simple and accurate analytical model can not be developed for this region of operation [9]. To obtain a

$$v_d(t) = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{\rm ol} + C_{\rm ox}/2}{C_L}\right)\cdot \exp\left[\frac{\beta U}{2C_L}\left(t - \frac{V_{\rm HT}}{U}\right)^2\right]\cdot\left\{\text{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{\rm HT}\right] - \text{erf}\left[\sqrt{\frac{\beta}{2UC_L}}(V_{\rm HT} - Ut)\right]\right\}. \tag{3}$$

simple analytical equation for the final charge injection error, an analytical MOS model proposed in [10] is used. This semi-empirical model which is also used by SPICE in the level 3 MOS model, shows good agreement with experimental data in weak and strong inversion [10] but is not quite as satisfactory in moderate inversion. However, there is good agreement between the charge injection error calculation using exact numerical me thods and the proposed model, indicating that the proposed model is sufficiently accurate for injection error calculations.

We assume that the I-V characteristics of a MOS transistor in the subthreshold region can be described by [10]

$$I_{\rm SUB} = I_0 \exp\left(\frac{V_{\rm GS} - V_{\rm on}}{nV_t}\right) \tag{5}$$

where $V_{\rm on}$ is the modified threshold voltage, given by

$$V_{\rm on} = V_T + nV_t \tag{6}$$

and n is the subthreshold slope factor

$$n = 1 + \frac{qN_{\rm FS}}{C'_{\rm ox}} + \frac{\gamma}{2\sqrt{\phi_B + V_{\rm SB}}}. \tag{7}$$

$C'_{\rm ox}$ is the oxide capacitance per unit gate area and V_t is the thermal voltage (kT/q). $N_{\rm FS}$ is the fast surface state density, $V_{\rm SB}$ is the source to substrate voltage and

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_a}}{C'_{\rm ox}}. \tag{8}$$

I_0 is the current in the strong inversion region for $V_{\rm GS} = V_{\rm on}$ [10]. For small values of $V_{\rm ds}$

$$I_0 = \beta(V_{\rm on} - V_T)V_{\rm ds} = n\beta V_t V_{\rm ds}. \tag{9}$$

I_0 depends on process parameters and transistor size.

B. The Gate–Source Capacitance Variation

In Sheu and Hu's simple model, the gate–source capacitance is considered to be $\frac{C_{\rm ox}}{2}$ above threshold and zero below threshold, respectively. Therefore, the variation of $C_{\rm gs}$ around threshold is ignored and also no inversion layer charges are assumed in subthreshold. In this modified model, two exponential functions are used to model the $C_{\rm gs}$ variation above and below the threshold voltage as follows (see Appendix):

$$C_{\rm gs} = \begin{cases} C_{\rm gsm} \exp\left(\frac{V_{\rm GS} - V_{\rm on}}{nV_t}\right) & V_{\rm GS} < V_{\rm on} \\ \frac{C_{\rm ox}}{2} - \left(\frac{C_{\rm ox}}{2} - C_{\rm gsm}\right) \exp\left(-\frac{V_{\rm GS} - V_{\rm on}}{kV_t}\right) & V_{\rm GS} \geq V_{\rm on} \end{cases} \tag{10}$$

where $C_{\rm gsm}$ is the gate–source capacitance when $V_{\rm GS} = V_{\rm on}$.

Fig. 4 shows that (10) is a better approximation to the $C_{\rm gs}$ variation than what has been used in Sheu and Hu's model.

C. The Analytical Models Above and Below Threshold

Similar to the analysis in Section II, two phases of operation are considered in this modified model during the turnoff transient. The new $C_{\rm gs}$ variation model (10) is used in both phases. In phase two, the subthreshold current effect is also added to this analysis.

In phase 1, following the method in Section II and using (10) to consider the $C_{\rm gs}$ variation above threshold results in a differential equation describing the circuit when ($V_G > V_S + V_{\rm on}$). The equation has an analytical solution given by

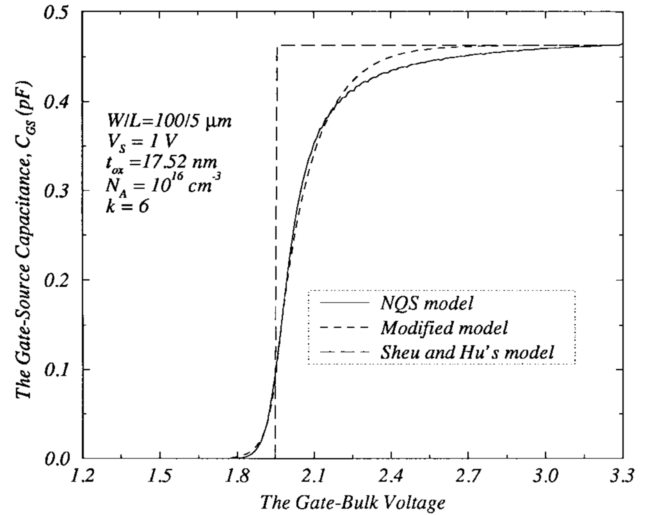


Fig. 4. The gate–source capacitance approximation.

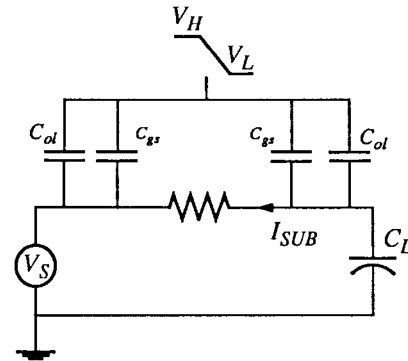


Fig. 5. Circuit model in the subthreshold region.

$$\begin{aligned} v_d(t) = &-\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{\frac{C_{\rm ox}}{2} + C_{\rm ol}}{C_L}\right)\exp\left[\frac{\beta U}{2C_L}\left(t - \frac{V_{\rm HT}}{U}\right)^2\right] \\ &\cdot\left\{\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{\rm HT}\right]\right. \\ &\left.-\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}(V_{\rm HT} - Ut)\right]\right\} \\ &+\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{\frac{C_{\rm ox}}{2} - C_{\rm gsm}}{C_L}\right) \\ &\cdot\exp\left[\frac{\beta U}{2C_L}\left(t - \frac{V_{\rm HT}}{U}\right)^2\right] \\ &\cdot\left\{\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\left(\frac{UC_L}{kV_t\beta} + V_{\rm HT}\right)\right]\right. \\ &\left.-\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\left(\frac{UC_L}{kV_t\beta} + V_{\rm HT} - Ut\right)\right]\right\}. \end{aligned} \tag{11}$$

The second term of (11) is due to the variation of $C_{\rm gs}$ around threshold. This term is less significant at smaller $\frac{UC_L}{kV_t\beta}$.

In the second phase ($V_G \leq V_S + V_{\rm on}$), the circuit to be analyzed is shown in Fig. 5.

Using (5) and (10), the differential equation describing the circuit can be derived as

$$\frac{dv_d}{dt} = -\left(\frac{C_{\rm ol}}{C_L} + \frac{C_{\rm gsm}}{C_L}\exp\left(\frac{V_{\rm GS}-V_{\rm on}}{nV_t}\right)\right)U - \frac{\beta n V_t}{C_L}\exp\left(\frac{V_{\rm GS}-V_{\rm on}}{nV_t}\right)v_d \tag{12}$$

where

$$V_{\rm GS} = V_H - V_S - Ut. \tag{13}$$

Substituting (13) into (12), the error voltage is found from the solution of the differential equation

$$\frac{dv_d}{dt} = -\frac{C_{\rm ol}}{C_L}U - \left(\frac{C_{\rm gsm}}{C_L}U + \frac{\beta n V_t}{C_L}v_d\right) \cdot \exp\left(\frac{V_{\rm HT}-nV_t}{nV_t}\right)\exp\left(-\frac{Ut}{nV_t}\right) \tag{14}$$

where

$$V_{\rm HT} = V_H - V_S - V_T. \tag{15}$$

Equation (14) has an exact solution of the form

$$v_d(t) = \frac{nV_t C_{\rm ol}}{C_L}e^Z[{\rm Ei}(Z_0) - {\rm Ei}(Z)] - \frac{C_{\rm gsm}U}{\beta n V_t}[1 - e^{Z-Z_0}] + e^{Z-Z_0}v_d(t_0) \tag{16}$$

where

$$Z = \frac{\beta (nV_t)^2}{UC_L}\exp\left(-\frac{U}{nV_t}(t-t_0)\right) \tag{17}$$

$$Z_0 = \frac{\beta (nV_t)^2}{UC_L} \tag{18}$$

and $v_d(t_0)$ is found from (11). Equation (16) is valid in the subthreshold region $(t \geq t_0)$ until the gate voltage reaches V_L $(t = t_f)$, where

$$t_0 = \frac{V_{\rm HT} - nV_t}{U} \tag{19}$$

and

$$t_f = \frac{V_H - V_L}{U}. \tag{20}$$

Ei is the exponential integral function defined by [11]

$${\rm Ei}(Z) = \int_Z^{\infty} \frac{e^{-y}}{y}dy \tag{21}$$

where y is a dummy variable.

Evaluating the exponential integral at the point associated with time t $(t \geq t_0)$ gives the output error voltage caused by the transistor in this region of operation. The final output error voltage can be calculated by substituting t_f into (16) and (17).

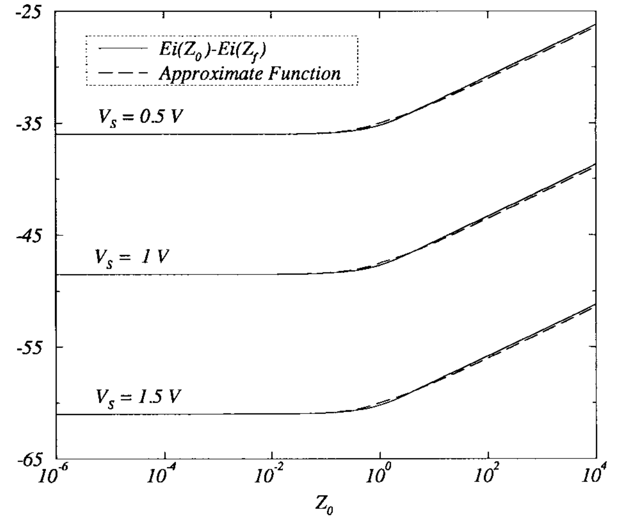


Fig. 6. $[{\rm Ei}(Z_0) - {\rm Ei}(Z_f)]$ and its approximate function.

IV. Approximate Analytical Model

An exact solution using the exponential integral requires numerical calculations. To obtain a simple analytical equation for the final output error voltage, an approximation is developed for $[{\rm Ei}(Z) - {\rm Ei}(Z_0)]$.

From (21), it can be seen that

$$[{\rm Ei}(Z_0) - {\rm Ei}(Z)] = \int_{Z_0}^{Z} \frac{e^{-y}}{y}dy. \tag{22}$$

It turns out that approximating $\frac{e^{-y}}{y}$ with e^{-y} and $\frac{1}{y}$ for y greater than and less than unity, respectively, gives an excellent approximation to the exact solution of (22) for $Z \ll 1$. Making these approximations results in the following limits:

$$[{\rm Ei}(Z_0) - {\rm Ei}(Z)] \approx \ln(Z) + (e^{-Z_0} - e^{-1}) \quad Z_0 \gg 1$$
$$[{\rm Ei}(Z_0) - {\rm Ei}(Z)] \approx \ln\left(\frac{Z}{Z_0}\right) \quad Z_0 \ll 1. \tag{23}$$

which are valid provided $Z \ll 1$.

A smooth transition between the two solutions given in (23) can be made by using the following form to express the integral of (22):

$$[{\rm Ei}(Z_0) - {\rm Ei}(Z)] \approx \ln\left[\left(1 + \frac{1}{Z_0}\right)Z\right] + e^{-e^{-Z_0}} - e^{-1}. \tag{24}$$

For our region of operation, Z_0 can be greater or less than unity, depending on the value of U. However, the value of Z at t_f (Z_f) is always much less than Z_0 and unity since

$$\frac{Z_f}{Z_0} = \exp\left(-\frac{V_S + V_T + nV_t - V_L}{nV_t}\right). \tag{25}$$

Fig. 6 shows the numerical evaluation of the exponential integral function along with (24) for the required values of Z_0 and Z_f when Z_f is obtained using (25). It is seen that (24) is a very close approximation to the exponential integral function over the range of Z_0 usually encountered in practice.

Substituting (24) into (16) and evaluating the time it takes for the gate voltage to reach V_L $(t = t_f)$, the final output

error voltage is determined to be

$$v_{\rm nf} = \frac{nV_tC_{\rm ol}}{C_L}\left\{\ln\left[\left(1+\frac{1}{Z_0}\right)Z\right] + e^{-e^{-Z_0}} - e^{-1}\right\} - \frac{C_{\rm gsm}U}{\beta nV_t}[1-e^{-Z_0}] + e^{-Z_0}v_d(t_0). \tag{26}$$

Substituting all the parameters, (26) can be written as

$$\begin{aligned} v_{\rm nf} &= e^{-(nV_t)^2\beta/2UC_L}v_d(t_0) \\ &\quad - \frac{C_{\rm ol}}{C_L}(V_S+V_T+nV_t-V_L) \\ &\quad + \frac{C_{\rm ol}}{C_L}nV_t\left\{\ln\left[1+\frac{\beta(nV_t)^2}{UC_L}\right] + \exp\left(-e^{-(nV_t)^2\beta/UC_L}\right) - e^{-1}\right\} \\ &\quad - \frac{C_{\rm gsm}U}{\beta nV_t}\left(1-e^{-(nV_t)^2\beta/UC_L}\right) \end{aligned} \tag{27}$$

where $v_d(t_0)$ can be calculated from (11).

The first and second terms in (27) correspond to the errors caused by the gate–oxide overlap capacitances when the transistor is in strong and weak inversion, respectively. The third term is the contribution of the subthreshold current to the cancellation of the error caused by the overlap capacitance in weak inversion. The last term is the error due to the inversion layer charge injection in the weak inversion region which decreases at the lower gate voltage falling rates. At high voltage falling rates, since the channel charge is divided equally between the source and drain, this term saturates at $\frac{C_{\rm gsm}nV_t}{C_L}$. Equation (27) then provides a simple and quite accurate analytical model for switch induced error voltage. The model is useful in describing the functional dependence of the error voltage on circuit and process parameters.

Equation (27) can be further simplified at high and low gate voltage falling rates. At high falling rates ($V_{\rm HT}^2\beta/2C_L \ll U$)

$$\begin{aligned} v_{\rm nf} &\simeq -V_{\rm HT}\left(\frac{C_{\rm ox}/2+C_{\rm ol}}{C_L}\right)\left(1-\frac{\beta V_{\rm HT}^2}{6UC_L}\right) \\ &\quad + V_{\rm HT}\left(\frac{C_{\rm ox}/2-C_{\rm gsm}}{C_L}\right) \\ &\quad \cdot\left(1-\frac{\beta}{6UC_L}\left[3\left(\frac{UC_L}{kV_t\beta}\right)^2 + 3V_{\rm HT}\left(\frac{UC_L}{kV_t\beta}\right) + V_{\rm HT}^2\right]\right) \\ &\quad - \frac{C_{\rm ol}}{C_L}(V_S+V_T+nV_t-V_L) - \frac{C_{\rm gsm}nV_t}{C_L} \end{aligned} \tag{28}$$

and at low falling rates ($V_{\rm HT}^2\beta/2C_L \gg U$)

$$\begin{aligned} v_{\rm nf} &\simeq -\frac{C_{\rm ol}}{C_L}(V_S+V_T+nV_t-V_L) \\ &\quad + \frac{C_{\rm ol}}{C_L}nV_t\left\{\ln\left[\frac{\beta(nV_t)^2}{UC_L}\right]\right\}. \end{aligned} \tag{29}$$

A comparison of (29) with Sheu and Hu's results at low falling rates [2] shows that the first term of (27) corresponding to the error caused by the injected charge above the threshold voltage has disappeared. In addition, the second term of (29), which is also due to the subthreshold current, decreases the final error voltage. At high falling rates, the subthreshold current effect is negligible and the contribution of the channel charges in the subthreshold region to the final error saturates at $\frac{C_{\rm gsm}nV_t}{C_L}$.

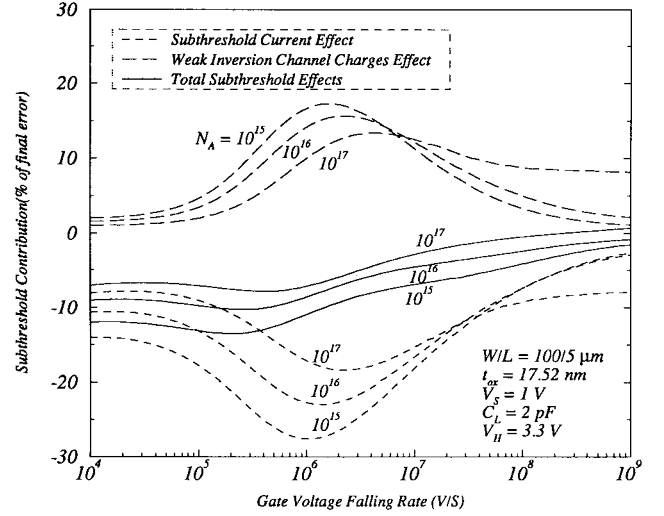


Fig. 7. Normalized subthreshold effects with respect to the gate voltage falling rate for different substrate dopings.

V. Dependence on Process and Electrical Parameters

In the weak inversion region, the effects of the subthreshold current and inversion layer charges on the charge-induced error depend on the circuit and process parameters. In (27) the third term which represents the subthreshold current effect, is independent of the input voltage signal level. As a result, at higher input voltage signal levels, as the total charge-induced error decreases, the subthreshold effect becomes more important. The last term in (27) indicates that the effect of the inversion layer charge in the weak inversion region is more significant at moderate gate voltage falling rates. In general, the exponential terms in (27) show that the lower the gate voltage falling rate, the more significant are the effects of the weak-inversion characteristics of the transistor.

Fig. 7 shows the contribution of the last two terms of (27) to the final charge induced error as a function of gate voltage falling rate. As can be seen, at all substrate dopings, the subthreshold current effect and the weak inversion channel charge effect cancel each other partially. However, as the falling rate decreases, ignoring the subthreshold effects can cause a higher error in the output voltage than that calculated using Sheu and Hu's model. Fig. 8 shows the subthreshold effects for various gate oxide thickness values.

The importance of the subthreshold effects with respect to the load capacitance is depicted in Fig. 9.

As can be seen, the subthreshold effect in an analog switch is important when larger transistor sizes, lower load capacitances, lower substrate dopings, smaller gate oxide thickness values and lower gate voltage falling rates are used.

VI. A Nonquasi-Static (NQS) Model

It has been shown in [6] and [7] that a nonquasi-static model can accurately predict the channel charge injection error. To check the approximate method proposed in the previous section, an NQS model based on [7] was used. All models were evaluated numerically using MATLAB.

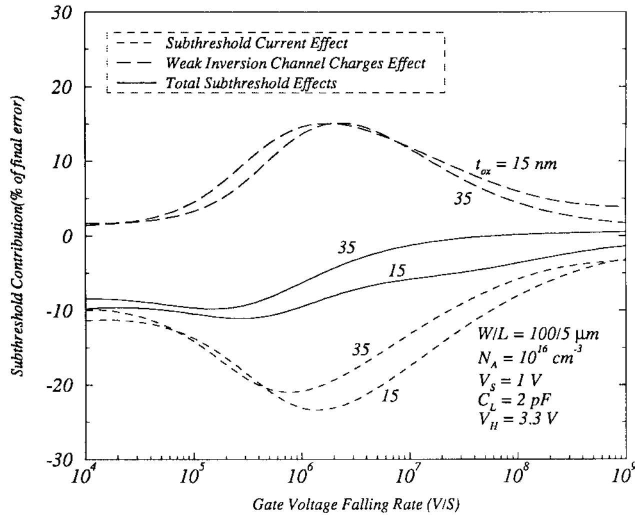


Fig. 8. Normalized subthreshold effects with respect to the gate voltage falling rate for different gate oxide thickness values.

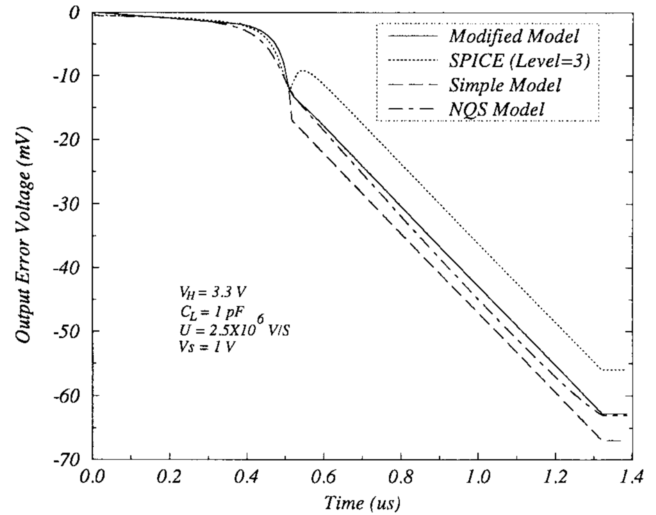


Fig. 10. Comparison of the output error voltage using different models.

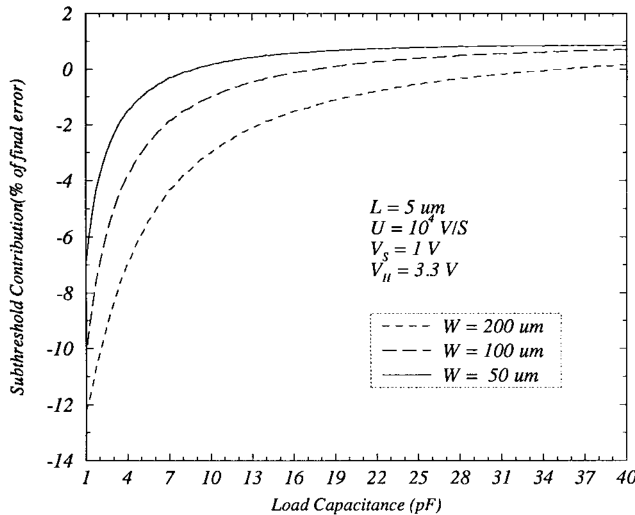


Fig. 9. Normalized subthreshold effect with respect to the load capacitance for different transistor widths.

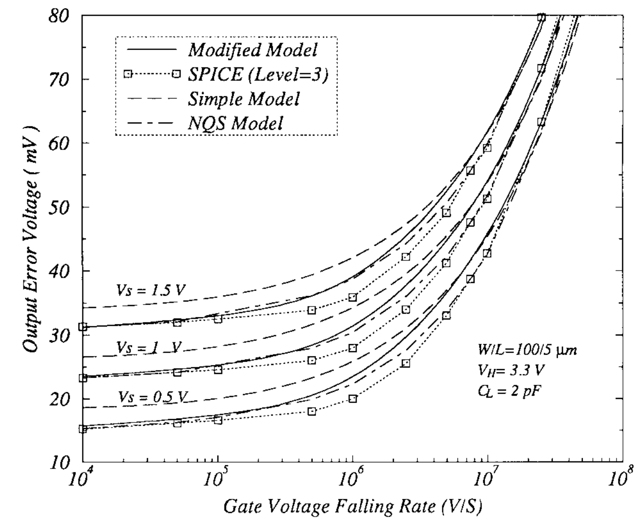


Fig. 11. Comparison of the different model results of the output error voltage as a function of the gate voltage falling rate.

In the NQS model, the transistor current continuity equation is solved approximately and analytical equations are derived for the node charges using the charge-sheet formulation. All the voltages and currents can be derived from these charges. This model includes the subthreshold current since the general partial differential equation for the channel inversion charge layer is solved. Excellent agreement has been reported between this model and various numerical simulators [7].

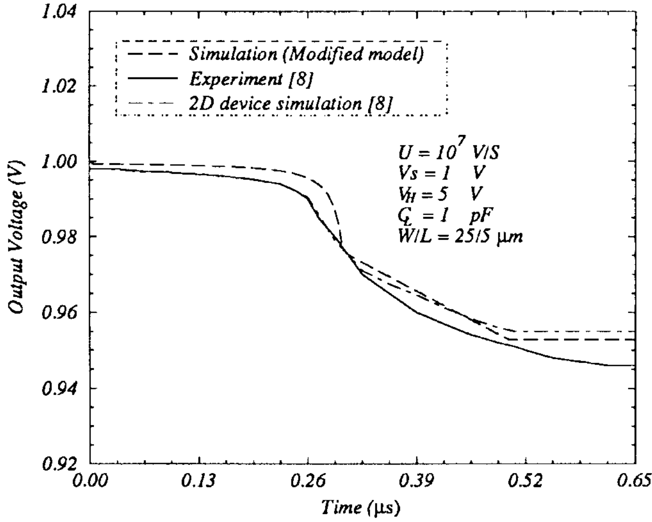
VII. Simulation Results

Fig. 10 shows the transient analysis of an analog switch with $W = 100$ μm and $L = 5$ μm. The model parameters of a commercial process were chosen as the simulation parameters where $N_A = 3.23 \times 10^{16}$ cm^{-3}, $T_{\rm ox} = 175$ Å, $N_{\rm FS} = 820 \times 10^9$ cm^{-2} V^{-1}, $V_{\rm FB} = -0.425$ V and the gate overlap capacitance is 2.74×10^{-10} farad per transistor width (m). The SPICE and simple model suggested by Sheu and Hu begin to deviate from the modified and NQS models in the subthreshold region $(t \geq 0.5$ μs). The final output error voltage for the different gate voltage falling rates is shown in Fig. 11. The modified and NQS models are in very good agreement over the range of gate voltage falling rates illustrated. Since the SPICE model (Level-3) considers only subthreshold current and ignores the inversion layer charge in the weak inversion region, it fails to correctly predict the final output error voltage at moderate gate voltage falling rates.

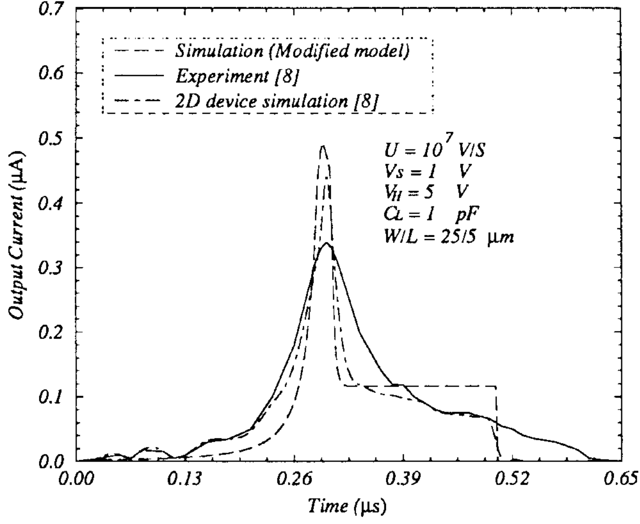
Fig. 12(a) and (b) compares the experimental and simulated results published in [8] with the modified model presented in this paper, and show the capability of this model to predict the charge induced output error voltage. The model parameters used were those presented in [8]. Since $N_{\rm FS}$ and $V_{\rm FB}$ were not specified, the abovementioned process values were chosen for these parameters. The results are not particularly sensitive to the values chosen.

VIII. Effect of Source Capacitance

The general equations for the output error voltage in the presence of finite source capacitance have been derived in



(a)



(b)

Fig. 12. Comparison of simulated and experimental results [8].

[2], [3] and [4]. By following the derivation described in Section III, the subthreshold effects can be added to these equations. However, the final differential equations can only be solved numerically. Fig. 13 shows the contribution of the subthreshold effects to the final error for various C_S/C_L ratios. The source resistance (R_S) is assumed infinitely large. As can be seen, the subthreshold effects are more significant for higher C_S/C_L ratios, where a relatively higher voltage is developed between the source and drain of the transistor.

IX. Conclusion

A simple model based on Sheu and Hu's model for analysis of the charge injection error which takes into account subthreshold effects has been described. An approximation has also been proposed to simplify the final error voltage calculation. The model was compared to SPICE and NQS models as well as recently published experimental results. Excellent agreement was achieved in all cases. The modified

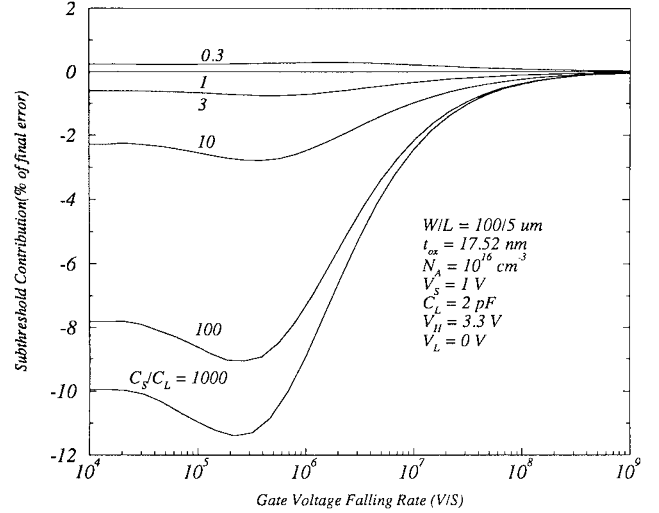


Fig. 13. Normalized subthreshold effect with respect to the gate voltage falling rate for different source–load capacitance ratios.

model provides physical insight into the effects of varing parameters in switching circuits in the weak inversion region.

Appendix
The Gate–Source Capacitance Variation in an MOS Switch

Charge neutrality in a MOS transistor results in

$$Q_G = Q_I + Q_B \tag{30}$$

where Q_G is the total gate charge, Q_I is the inversion layer charge and Q_B is the total bulk charge. Q_G and Q_B are given by

$$\begin{aligned} Q_G &= -C_{\text{ox}}(V_G - V_{\text{FB}} - \psi_S) \\ Q_B &= -C_{\text{ox}}\gamma\sqrt{\psi_S}. \end{aligned} \tag{31}$$

V_{FB} is the flat band voltage and ψ_S is the surface potential at the source given by

$$\psi_S = V_G - V_{\text{FB}} - \gamma\sqrt{\psi_S + V_t e^{(\psi_S - 2\phi_F - V_S)/V_t}}. \tag{32}$$

Based on the drain–source voltage, Q_I is divided into source and drain charges (Q_S and Q_D). For small V_{DS} where $Q_S \simeq Q_D$, the gate charges can be written as

$$Q_G = 2Q_S + Q_B. \tag{33}$$

The gate–source capacitance is defined by

$$C_{\text{gs}} = -\frac{dQ_S}{dV_G}. \tag{34}$$

Substituting (30)–(33) into (34), yields C_{gs} at the threshold voltage where $\psi_S = 2\phi_F + V_S$ to be

$$\begin{aligned} C_{\text{gsm}} &= C_{\text{gs}}(\psi_S = 2\phi_F + V_S) \\ &= \frac{1}{1 + \sqrt{2\phi_F + V_S}/\gamma}\left(\frac{C_{\text{ox}}}{4}\right). \end{aligned} \tag{35}$$

Above the threshold voltage C_{gs} increases with respect to the gate–source voltage and saturates at $\frac{C_{\text{ox}}}{2}$. However, the

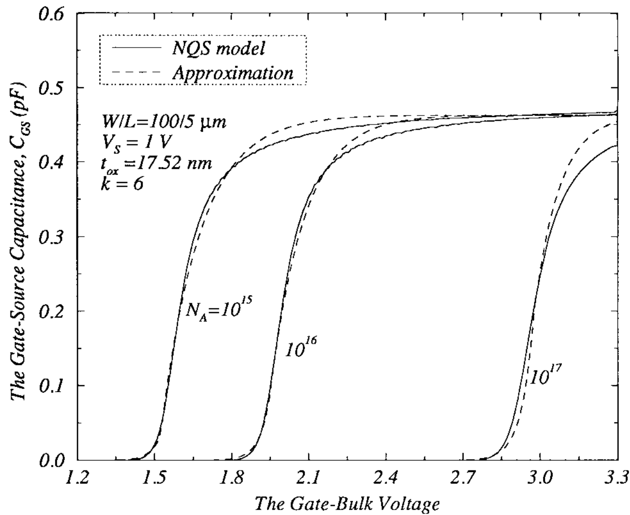


Fig. 14. The gate–source capacitance approximation for different substrate dopings.

inversion layer charges decrease exponentially with respect to the gate–source voltage in the weak inversion region [9]. Since there are negligible variations of the depletion region charges below threshold, the total gate charges and consequently the gate–source capacitance $(C_{\rm gs})$ decrease exponentially with respect to the gate–source voltage in the weak inversion region. In other words, in weak inversion

$$C_{\rm gs} \propto \exp\left(\frac{V_{\rm GS}-V_{\rm on}}{nV_t}\right). \tag{36}$$

Therefore, $(C_{\rm gs})$ can be approximated by two exponential functions above and below the threshold voltage as follows:

$$C_{\rm gs} = \begin{cases} C_{\rm gsm} \exp\left(\frac{V_{\rm GS}-V_{\rm on}}{nV_t}\right) & V_{\rm GS} < V_{\rm on} \\ \frac{C_{\rm ox}}{2} - \left(\frac{C_{\rm ox}}{2} - C_{\rm gsm}\right) \exp\left(-\frac{V_{\rm GS}-V_{\rm on}}{kV_t}\right) & V_{\rm GS} \geq V_{\rm on}. \end{cases} \tag{37}$$

In (37), k is a fitting factor between 5 and 10 for the practical range of substrate dopings and gate oxide thickness.

A comparison of (37) and the accurate NQS model results for different substrate dopings (Fig. 14) shows that (37) is a good approximation of $C_{\rm GS}$ for small drain–source voltages.

REFERENCES

[1] D. MacQuigg, "Residual charge on a switched capacitor," *IEEE J. Solid-State Circuits*, vol. SSC-18, pp. 811–813, Dec. 1983.

[2] B. J. Sheu and C. Hu, "Switched-induced error voltage on a switched capacitor," *IEEE J. Solid-State Circuits*, vol. SSC-19, pp. 519–525, Aug. 1984.

[3] J. H. Sheu, M. Patil, and B. J. Sheu, "Modeling charge injection in MOS analog switches," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 214–216, Feb. 1987.

[4] B. J. Sheu, J. H. Shieh, and M. Patil, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SSC-22, pp. 277–281, Apr. 1987.

[5] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. SSC-22, pp. 1091–1097, Dec. 1987.

[6] H. J. Park, P. K. Ko, and C. Hu, "A nonquasi-static MOSFET model for SPICE-transient analysis," *IEEE Trans. Electron Devices*, vol. 36, pp. 561–575, Mar. 1989.

[7] ——, "A charge conserving nonquasi-static (NQS) MOSFET model for SPICE transient analysis," *IEEE Trans. Computer-Aided Design*, vol. 10, pp. 629–642, May 1991.

[8] M. J. Chen, Y. B. Gu, T. Wu, P. C. Hsu, and T. H. Liu, "Weak inversion charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. 30, pp. 604–606, May 1995.

[9] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[10] R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistor in low-voltage circuits," *IEEE J. Solid-State Circuits*, vol. SSC-7, pp. 146–153, Apr. 1972.

[11] E. Kreyszig, *Advance Engineering Mathematics*. Wiley, 1967.

Saeed Aghtar (S'96) was born in Isfahan, Iran, in 1967. He received the B.Sc. degree in electrical engineering from the Isfahan University of Technology, and the M.Sc. degree in electrical engineering from Tehran University, Tehran, Iran, in 1989 and 1992, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Calgary, Calgary, Alta., Canada.

His current research interests are precision analog-to-digital conversion, current mode circuits, and electronic instrumentation.

J. W. Haslett (M'64–SM'79) was born in Saskatchewan, Canada, on September 27, 1944. He received the B.Sc. degree in electrical engineering from the University of Saskatchewan, Saskatoon, in 1966, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Calgary, Calgary, Alta., Canada, in 1968 and 1970, respectively.

In 1970, he joined the Department of Electrical Engineering, University of Calgary, where he is currently Professor and head of the department. His current research interests include optical imaging systems for spacecraft applications, instrumentation systems related to drill stem testing of oil and gas wells, high-temperature semiconductor device behavior, and the design of analog and digital VLSI circuits.

Dr. Haslett is a member of the Association of Professional Engineers, Geologists, and Geophysicists of Alberta, the Canadian Astronomical Society, the Canadian Society of Exploration Geophysicists, and the American Society of Engineering Education.

F. N. Trofimenkoff (M'63–SM'69) was born in Veregin, Saskatchewan, Canada, on August 10, 1934. He received the B.E. degree in engineering physics and the M.Sc. degree in physics, both from the University of Saskatchewan, Saskatoon, in 1957 and 1959, respectively. He was awarded an Athlone Fellowship in 1959 and received the Ph.D. degree in electrical engineering (semiconductor device physics) from the University of London, the Imperial College of Science and Technology, London, U.K., in 1962.

From 1957 to 1959, he worked on instrumentation for accurate humidity measurement in the Division of Building Research, the National Research Council of Canada, and from 1962 to 1966, he was an Assistant Professor of Electrical Engineering, University of Saskatchewan. In 1966, he joined the Department of Electrical Engineering, University of Calgary. His current research interests are in the circuits and devices area and in instrumentation related to the petroleum industry.

Dr. Trofimenkoff is a member of the Association of Professional Engineers, Geologists, and Geophysicists of Alberta, the Engineering Institute of Canada, the Canadian Association of Physicists, and the American Society for Engineering Education.