A $0.18\mu m$ CMOS Bluetooth Frequency Synthesizer for Integration with a Bluetooth SOC Reference Platform

Bogdan A. Georgescu†,*, Joshua K. Nakaska†,*, Robert G. Randall†,*, James W. Haslett†,*
†University of Calgary, Department of Electrical and Computer Engineering
RFIC Research Group and the ATIPS Laboratory
*TR*Labs*
haslett@enel.ucalgary.ca

Abstract

*Bluetooth is a communications standard targeting short-range wireless communications with data rates of 1Mb/s at 10m distance. To encourage Canadian universities to pursue this commercially promising standard the Canadian Microelectronics Corporation is providing the intellectual property for a Bluetooth SOC Reference Platform. This platform does not currently include an RF transceiver core. This work describes a research effort made at the University of Calgary to build a compatible RF transceiver core in a CMOS 0.18μm process. A brief Bluetooth specification translation process to derive the frequency synthesizer system specifications is presented. A pilot PCB Bluetooth frequency synthesizer is presented together with specific measurements made at NEWT, TR*Labs*' new test and measurement facility. Finally, a fully integrated Bluetooth frequency synthesizer implemented in a CMOS 0.18μm process is presented.*

1. Introduction

The Bluetooth standard was designed to achieve cost-effective wireless communications providing a data rate of 1Mb/s at 10m distance. Destined to be primarily a flexible cable replacement, growth in the Bluetooth arena has resulted in over 10 million integrated circuit units shipped by Philips alone [7]. The specifications for the standard have been relaxed in order to facilitate a fully integrated chipset solution. Therefore this standard is very suitable for an SOC approach. Several platforms are already available on the market for Bluetooth SOC rapid development and prototyping to shorten design cycles and limit the scope of design teams. These Bluetooth intellectual property (IP) cores provide protocol stack functionality in the form of software and synthesizable hardware description language (HDL).

Although much of the Bluetooth standard has been commercially implemented, work is still needed to improve the baseband physical radio, in integrated circuit form in terms of: production costs, power consumption, and implementation in the newer smaller feature size processes. To facilitate Bluetooth research in Canadian universities, the Canadian Microelectronics Corporation (CMC) is providing the IP for the Bluetooth SOC Reference Platform (BSRP) acquired from Tality Corporation[1].

In this paper a brief overview of the BSRP is given (Section 2) and a brief architecture discussion of the radio frequency (RF) transceiver is made (Section 3). Then, in Section 4, the translation from standard specifications to RF transceiver specifications is presented.

In Section 5 the design for a printed circuit board (PCB) frequency synthesizer using National Semiconductor's Easy-PLL design service is shown together with verified performance measurements.

In Section 6 the design for a fully integrated Bluetooth frequency synthesizer implemented in a $0.18\mu m$ CMOS process is presented. The frequency synthesizer forms a part of the RF transceiver that will be integrated with the BSRP.

2 Bluetooth SOC Reference Platform

The CMC development platform is composed of two design components: the Bluetooth SOC Reference Platform (BSRP, [1]), and a software protocol engine. Between these two main components, CMC clients have access to synthesizable IP cores in the form of re-configurable VHDL and Verilog HDL, and a software development infrastructure. These cores provide much of the functionality and components of the Bluetooth protocol stack (Fig. 1, [2]) down to the baseband layer.

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[1] Tality Corporation, formerly a subsidiary of Cadence Design Systems, Inc. has since returned to Cadence Design Systems, Inc. [4]

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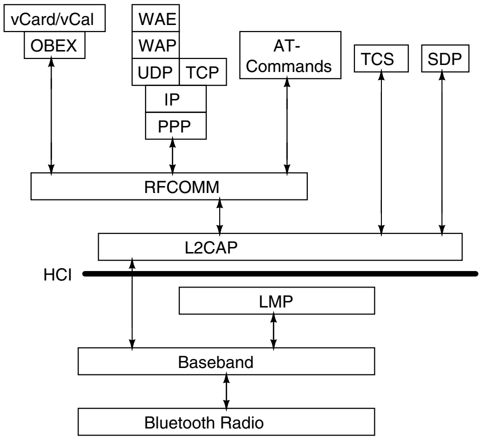

Figure 1. Bluetooth Protocol Stack [2]

The BSRP provides the interface between the ARM microcontroller unit (MCU) and the AMBA[2] buses (Fig. 2, [1]). The AMBA advanced peripheral bus (APD) and advanced high-performance bus (AHB) further interface to the UART and other custom modules, and to the system and memory controllers.

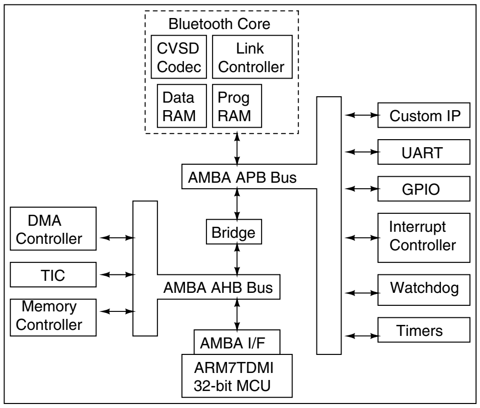

Figure 2. Bluetooth SOC Reference Platform

To summarize, CMC clients have access to the following: the BSRP core, the baseband controller, the AMBA bus and bus interface, and an IEEE 802.3 compatible ethernet MAC.

The following components are not included in the BSRP platform: ARM's 32-bit RISC ARM7TDMI MCU core, an RF transceiver, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and external memory. This means that researchers are not in a position to realize a complete Bluetooth solution for further development. Current research at the University of Calgary on the Bluetooth RF transceiver is intended to help bridge this development gap.

3 RF Transceiver System Components

The Bluetooth RF transceiver requires several system components: a quadrature frequency synthesizer, a low noise amplifier (LNA), mixers to provide frequency translation from RF frequencies to baseband, and amplifiers (Fig. 3).

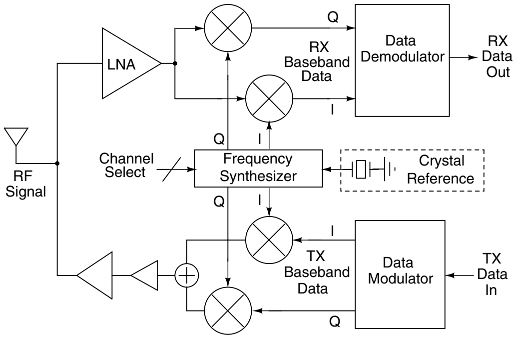

Figure 3. RF Transceiver

In addition to the RF transceiver, ADCs and DACs must also be designed.

4 Translating the Bluetooth Standard Specifications Into Radio Design Specifications

In designing the Bluetooth RF transceiver the first step is to extract the necessary system requirements from the standard. Figures of merit such as noise figure (NF), third order intercept point (IP3), spurious free dynamic range (SFDR) and synthesizer specifications need to be extracted. To ensure the standard requirements are met, sophisticated system simulations must be performed. An overview of simple procedures to estimate the main figures of merit is given.

4.1 Noise Figure Specifications

In [3] (Section 4.1, p.25) the actual receiver sensitivity level is defined as the input level for which a raw bit error rate of 0.1% is met. The requirement for a Bluetooth receiver is an actual sensitivity level of -70dBm or better. The receiver must achieve the -70dBm sensitivity level with any Bluetooth transmitter compliant to the transmitter specification given in [3] (Section 3, p.21).

The modulation characteristics for Bluetooth are Gaussian Frequency Shift Keying (GFSK) with BT=0.5 and a modulation index $MI = \frac{2\Delta f_{(SSB)}}{BW} = 0.28 \sim 0.35$, where 140kHz $< \Delta f_{(SSB)} <$ 175kHz is the frequency deviation.

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[2] AMBA is an open on-chip bus standard designed for SOC implementations.

To obtain a bit error rate of 0.1%, $\frac{S}{N} \approx 21dB$. This means the allotted noise floor is -91dBm. Since

$$P_{in,min} = -174\frac{dBm}{Hz} + NF + 10logB + \left(\frac{S}{N}\right)_{min} \quad (1)$$

where sensitivity $P_{in,min} = -70dBm$, $B = 1MHz$, $SNR_{min} = 21dB$, the Bluetooth receiver is required to achieve NF<23dB.

4.2 IP3 Specifications

In [3] (Section 4.4, p.26) regarding intermodulation characteristics, the required BER = 0.1%, must be met under the following conditions:

- The wanted signal at frequency f_0 with a power level of 6dB over the reference sensitivity level
- A static sine wave signal at f_1 with a power level of -39dBm
- A Bluetooth modulated signal at f_2 with a power of level of -39dBm

such that $f_0 = 2f_1 - f_2$ and $|f_2 - f_1| - n \times 1MHz$, where n can be 3, 4 or 5. The system must fulfill one of the three alternatives. The interference performance requires that the co-channel interference is 11dB [3] (Section 4.2, p.25). The third order products produced from signals in two adjacent channels are at the same frequency as the desired signal. This third order product should not cause a degradation in BER. Since the power in the *desired* channel is -64dBm, the third order product caused by $2f_1 - f_2 (= f_0)$ has to be 11dB below the desired signal to satisfy the co-channel interference requirements. Therefore we need:

$$-39dBm + G - 2X < -64dBm - 11dB + G \quad (2)$$

where G is the gain of the receiver and 2X is the difference between the third order products output power created by the 39dBm tones and the output power due to the tones themselves as shown in Fig. 4. This translates into X = 18dB and input referred $IP3 > -39dBm + 18dB = -21dBm$.

4.3 SFDR Specifications

The spurious free dynamic range (SFDR) is defined as the signal to noise ratio corresponding to the input amplitude at which the third order intermodulation product power just equals the noise power in decibels. Referring to Fig. 5,

$$3Y = -21 + G - (-114 + G + 23) \quad (3)$$

Thus $SFDR = 2Y = 46.7dB$.

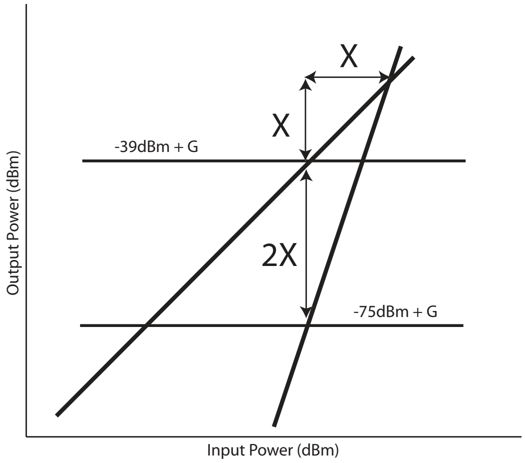

Figure 4. Third-Order Intermodulation

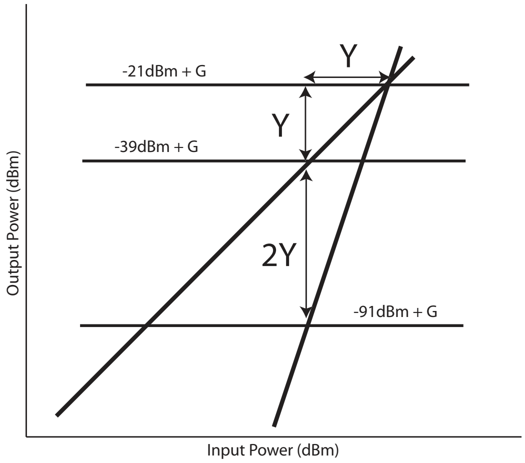

Figure 5. Spurious Free Dynamic Range

4.4 Synthesizer Settling Time

The synthesizer for a Bluetooth radio has to be able to provide frequencies from 2402MHz to 2480MHz in steps of 1MHz. The frequency tolerance is ±75kHz. Special requirements must be imposed on the settling time when the system hops. The standard specifications require the synthesizer to be able to hop 1600 times per second while delivering data packets. The bit duration is $1\mu s$ since the symbol rate is 1Mbps. The maximum number of bits of a standard packet is: $72_{(ACCESS\ CODE)} + 54_{(HEADER)} + 2745_{(PAYLOAD)} = 2871$.

In the worst case the settling time for 5 time slots each of duration $625\mu s \left(\frac{1}{1600\ hops/sec}\right)$ has to be less than (3125-2871) = $254\mu s$ [3] (Section 4.6, p.65). In reality this time has to be smaller to account for the 3-wire (DATA,CLK,ENABLE) control time of the synthesizer.

4.5 Synthesizer Spurious Response

To meet interference performance the spurs generated by the synthesizer have to be at a certain level below the carrier. The interference performance requires that the co-channel interference is 11dB [3] (Section 4.2, p.25).

For an offset of 1MHz the desired signal is -60dBm, 10 dB above the reference sensitivity level. An interferer may be as strong as -60dBm at 1MHz offset (0 dB above the desired signal). To satisfy the co-channel interference requirements, the power of a synthesizer spur at 1MHz from the carrier denoted X dBc, has to satisfy: $-60-(-60+X) > 11dB$ which yields $X(1MHz) < -11dBc$.

For an offset of 2MHz the desired signal is -60dBm, 10 dB above the reference sensitivity level. An interferer may be as strong as -30dBm at 2MHz offset (30 dB above the desired signal). To satisfy the co-channel interference requirements, the power of a synthesizer spur at 2MHz from the carrier denoted X dBc, has to satisfy: $-60-(-30+X) > 11dB$ which yields $X(2MHz) < -41dBc$.

For an offset of 3MHz the desired signal is -67dBm, 3 dB above the reference sensitivity level. An interferer may be as strong as -27dBm at 3MHz offset (40 dB above the desired signal). To satisfy the co-channel interference requirements, the power of a synthesizer spur at 3MHz from the carrier denoted X dBc, has to satisfy: $-67-(-27+X) > 11dB$ which yields $X(3MHz) < -51dBc$.

Therefore the most stringent requirement occurs when an interferer is at a 3 MHz offset.

5 Bluetooth Synthesizer PCB

To validate the measurement procedure and verify basic functionality a prototype PCB based Bluetooth synthesizer with discrete components was designed and fabricated using National Semiconductor's EasyPLL service. The lock time and spectral content of the frequency synthesizer were verified using the equipment and expertise of the Network for Emerging Wireless Technologies (NEWT) a newly opened wireless test and measurement center affiliated with TR*Labs*. The spectral content of the synthesizer, shown in Fig. 6, was measured using the Agilent E4440A spectrum analyzer. To measure the lock time, the synthesizer was programmed to hop and the output signal was down converted using the spectrum analyzer. The down converted time domain data was captured with an Agilent 54381B Infiniium oscilloscope and passed to Agilent's 89600 vector signal analyzer software, where an FM demodulation was used to capture the instantaneous frequency of the signal. In this way, the settling time for a maximal frequency jump was obtained, as shown in Fig. 7. These results show that the PCB based frequency synthesizer performance was compliant with the Bluetooth standard ($t_{lock} \approx 110\mu s < 254\mu s$).

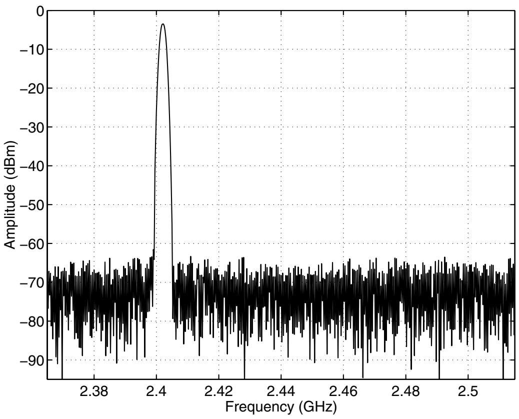

Figure 6. 2.402 GHz Spectrum Measurement

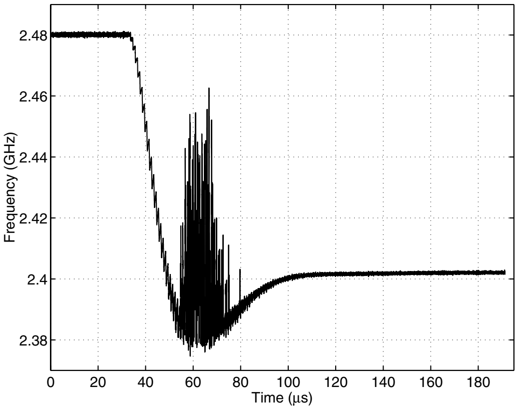

Figure 7. Lock Time Measurement

6 Integrated Frequency Synthesizer Design

The system architecture of the frequency synthesizer was similar to that used in [5], but with a smaller feature size process and a lower supply rail of 1.8V. An integer-N architecture utilized a 10 MHz crystal reference oscillator divided down 15 times to ≈ 666.667 kHz (Fig. 8). Since the actual transceiver is $1.5 \times f_{VCO}$, this leads to the required 1MHz Bluetooth channel spacing.

6.1 Loop Filter Design

The second-order loop filter was integrated using a resistor and two capacitor arrays (Fig. 9, [6]). The design equations are shown in Table 1. The capacitors were created using many high-density metal-insulator-metal (MIM) capacitors in parallel.

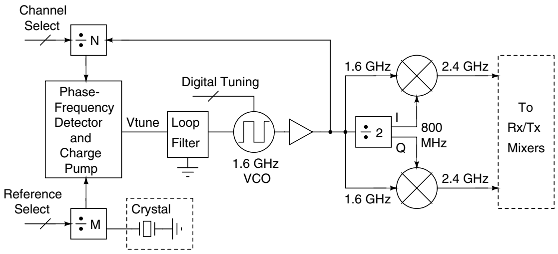

Figure 8. Frequency Synthesizer Block Diagram

Table 1. Loop Filter Parameters [6]

Parameter Description	Value
I_{qp}, Charge Pump Current	$100\mu A$
K_{VCO}, VCO Tuning Slope	$140\frac{MHz}{V}$
w_c, Filter Cutoff Frequency	$45kHz$
$R_z = \frac{2\pi \cdot N}{I_{qp} \cdot K_{VCO}} \cdot w_c$	$R_z \approx 304k\Omega$
$C_z = \frac{I_{qp} \cdot K_{VCO}}{2\pi \cdot N} \cdot \frac{\alpha}{w_c^2}$	$C_z \approx 256pF$
$C_p = \frac{I_{qp} \cdot K_{VCO}}{2\pi \cdot N} \cdot \frac{1}{\beta \cdot w_c^2}$	$C_p \approx 21pF$

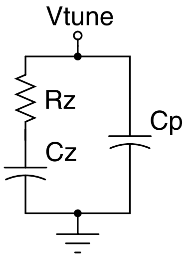

Figure 9. 2^{nd} Order Loop Filter

6.2 Mixers

Mixers were implemented using the configuration shown in Fig. 10. The inductively loaded mixer provided acceptable output spurious content.

6.3 VCO Circuit Design and Operation

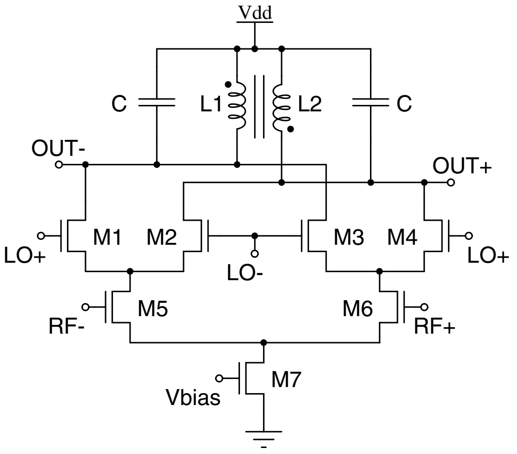

Figure 10. Gilbert Mixer with Transformer-Based Inductive Loading

The differential VCO was designed to have digital coarse tuning and analog fine tuning (Fig. 11). Coarse tuning of the VCO is provided, by supplying a 4-bit digital control word, which switches in additional capacitance. Source followers were used to buffer the VCO output signals.

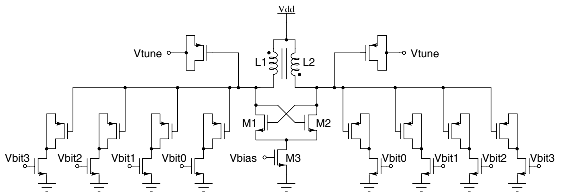

Figure 11. Differential Cross-Coupled CMOS VCO Core

Square spiral inductors in the LC-tank of the VCO were designed in a transformer configuration to provide enhanced phase noise performance.

6.4 Dividers

The divide-by-N function was developed using an RF prescaler and programmable counters (Fig. 12). The RF prescaler divides the incoming RF signal by either 15 or 16. In order to cover the Bluetooth frequency band, one programmable counter counts *P* from 0 to 159 (the program counter, *PC*), and another programmable counter counts *S* from 0 to a minimum of 13 and a maximum of 113 (the swallow counter, *SC*). In this case, the division ratio, *N* is: $N = (15 \times 159) + S + 2 = 2400 \sim 2500$. Therefore the entire 2.4GHz ISM frequency band may be utilized.

Divide-by-two circuits were used to divide down the 1.6GHz signal to 800MHz for mixing. These divide-by-two circuits were also used to generate the in-phase and

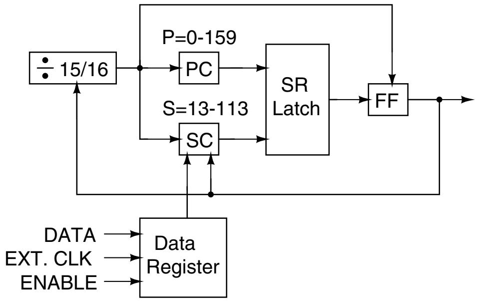

Figure 12. Prescaler Block Diagram

quadrature-phase output (and each of their respective differential signals). The divide-by-two circuit consisted of two connected latches in a master-slave configuration (Fig. 13) with a single phase-inversion in the loop.

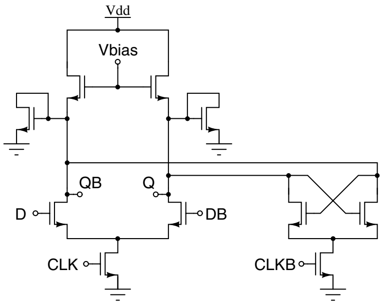

Figure 13. CMOS Latch

The crystal reference frequency divider was a programmable divider normally set to 15, but capable of division ratios from 1 to 31, to be flexible for additional input crystal frequencies.

6.5 Frequency Synthesizer Layout

The final frequency synthesizer layout (Fig. 14) had dimensions of $2015\mu m$ x $1715\mu m$. A large portion of the layout is dedicated to the integrated loop filter. Careful attention was paid to minimizing noise coupling through the power rails. Completely separate analog and digital power rails isolate the analog VCO and mixers from the digital logic devices.

7 Conclusions

This paper describes the design of a frequency synthesizer for integration with a Bluetooth SOC Reference Platform. A brief Bluetooth specification translation process to derive the frequency synthesizer system specifications was presented. A pilot PCB Bluetooth frequency synthesizer was demonstrated together with specific measurements made at NEWT. Finally, a fully integrated Bluetooth frequency synthesizer design in a CMOS $0.18\mu m$ technology which serves as a part of the Bluetooth RF transceiver was shown.

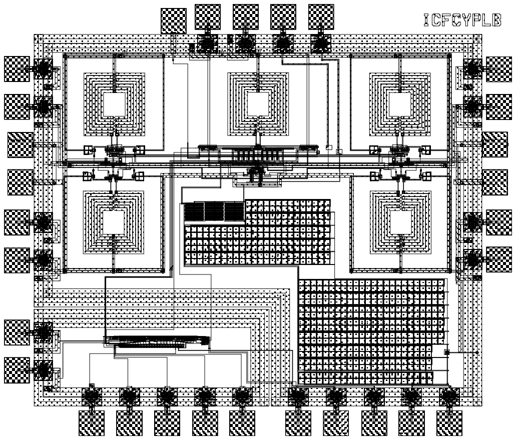

Figure 14. Frequency Synthesizer Layout

8 Acknowledgements

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