BiCMOS Adjustable Linear Current Mirror

A. K. Gupta, J. W. Haslett, and F. N. Trofimenkoff

Abstract— **Two novel BiCMOS adjustable gain linear current mirrors are presented. Variable gain is achieved by introducing a dc voltage into the control loop. Simulation and experimental results indicate that the gain is linear over several decades of signal current. The circuits are designed for maximum voltage swing with cascoded output to provide high output resistance.**

Index Terms— **Mirrors, BiCMOS.**

I. Introduction

VARIABLE gain current mirrors are used in a variety of analog signal processing applications such as active filters [1], D/A and A/D converters [2], current-mode signal processing circuits [3], optical centroid detectors [4], autozeroed operational amplifiers, etc. Adjustable current mirrors based on the log–antilog property of the bipolar transistor have been developed [1], [3], [5]. These current mirrors have good controllability and linearity over several decades of signal current. Although bipolar transistors have excellent log–antilog properties, they suffer from finite current gain β and dependence of β on collector current (the β degradation effect). In the circuits published to date, a small nonlinearity in the cascode output circuit is present due to finite β, to the β degradation effect of the bipolar transistor, and to the internal resistance of the control voltage source.

The proposed current mirrors [6] are designed with BiCMOS technology, and take advantage of the log–antilog property of the bipolar transistors and infinite gate resistance of the MOS transistors to achieve improved linearity. High output resistance is achieved using improved cascode circuits which facilitate maximum voltage swing.

II. Adjustable Current Mirror

The basic principle used to achieve an adjustable current mirror (ACM) is based on the log–antilog property of bipolar transistors. The addition of a constant term in the log transform results in a gain term in the antilog transform. This concept can be realized in two ways as shown in Figs. 1(a) [1] and (b) [5]. The internal resistance of the voltage source V_{CTRL} and the parasitic resistances of the transistors cause a nonlinearity in the transfer function at large signal currents. The realization of the concept as shown in Fig. 1(b) reduces the effect of the internal resistance of the voltage source by approximately two orders of magnitude. Two new circuits are presented based on this realization. These will be referred to as the base resistor adjustable current mirror and the active voltage source adjustable current mirror.

Manuscript received December 19, 1995; revised June 10, 1996. This work was supported by NSERC under Grants OGP0 007 776 and OGP0 003 382 and by the Canadian Microelectronics Corporation.

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Publisher Item Identifier S 0018-9200(97)00400-9.

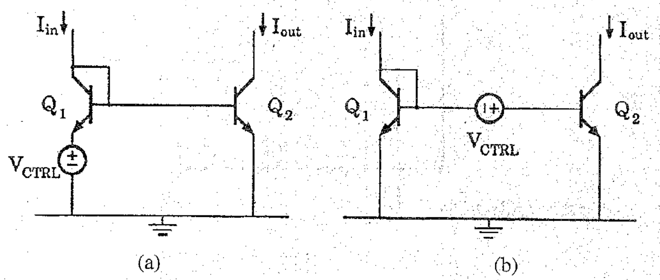

Fig. 1. Two different realizations of the adjustable current mirror.

A. Base Resistor Adjustable Current Mirror

One method of implementing the circuit in Fig. 1(b) is shown in Fig. 2(a). The realization of the voltage source V_{CTRL} is achieved by the resistances R_b and the current sources I_{CTRL} and I_{CONST} [5]. The gain is adjusted by controlling current I_{CTRL}. The sum of the base currents, the control current I_{CTRL}, and the bias current I_{CONST} flows through the MOSFET M_1 without affecting the input current. The resistances R_b are in the range of a few hundred ohms, making the circuit easy to fabricate in monolithic form. Nonlinearity is introduced by the finite parasitic emitter and base resistances of transistors Q_1 and Q_2 and resistances R_b. The magnitude of resistances R_b and controlling current I_{CTRL} determine the tradeoff between nonlinearity and power dissipation.

To increase the output resistance, the cascode configuration can be used. Fig. 2(b)–(f) shows different cascode circuit implementations with the basic base resistor ACM. MOSFET's M_2 and M_3, as shown in Fig. 2(b), can be used in the cascode configuration although the low g_m of the MOSFET's and the large voltage drop between the gate and source make this alternative less attractive. NPN transistors Q_3 and Q_4, as shown in Fig. 2(c), can also be used in the cascode configuration to provide high output resistance. In many CMOS technologies, V_{gs} for a moderate drain current is generally much larger than $V_{BE_{ON}}$ of the bipolar transistor. Using this fact, the cascode configuration shown in Fig. 2(c) can be modified as shown in Fig. 2(d) to provide larger input voltage swing. The geometry of the MOSFET M_1 should be chosen carefully to bias the circuit properly for the maximum specified signal current and the minimum V_{TO} of M_1.

The current gain of the current mirrors shown in Fig. 2(c) and (d) will depend on the β of transistor Q_4 because the base current flowing through Q_4 does not get amplified, but is subtracted from the amplified current. The β degradation effect causes a change in the current gain which introduces a significant amount of nonlinearity. Another MOSFET, M_2,

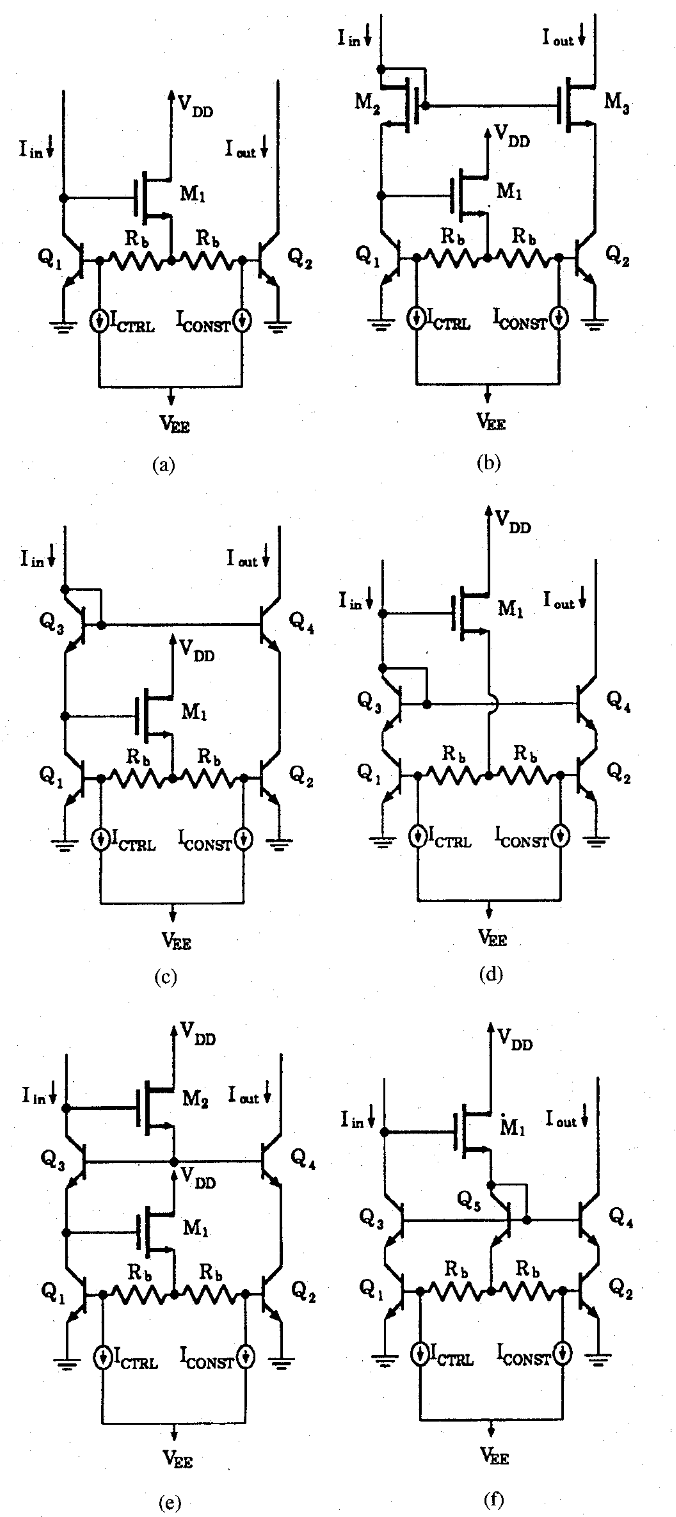

Fig. 2. Base resistor adjustable current mirror.

can be used to provide base currents to Q_3 and Q_4 as shown in Fig. 2(e) to decrease the β degradation effect. This circuit can be modified to increase the voltage swing as shown in Fig. 2(f). The geometry of Q_5 should be chosen so that Q_1 and Q_2 are biased in the forward active region for the maximum specified signal current. This circuit has very little β degradation effect, maximum output resistance, and moderate voltage swing.

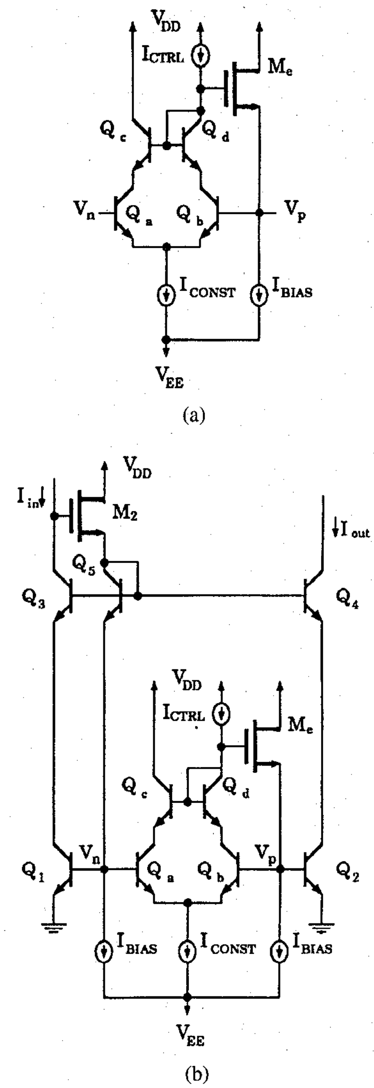

Fig. 3. Active voltage source adjustable current mirror. (a) Active voltage source. (b) Adjustable current mirror.

B. Active Voltage Source Adjustable Current Mirror

In the base resistor ACM, the control voltage source is realized by a passive resistor and a current source. The internal resistance of this type of voltage source is equal to the resistance of the resistor used. To achieve low internal resistance, the active voltage source shown in Fig. 3(a) can be used as the control voltage source. The control voltage is controlled by the current source I_{CTRL}. By choosing suitable bias currents and geometries of the MOSFET M_e, the internal resistance can be made as small as 1–10 Ω. If this voltage source is used in the ACM scheme shown in Fig. 1(b), the nonlinearity at the high signal current levels will be dominated by the parasitic resistances of Q_1 and Q_2. Fig. 3(b) shows the adjustable current mirror circuit using the active voltage source and the β degradation immune cascode circuit.

III. ANALYSIS

Base resistor adjustable current mirrors with and without the β degradation immune cascode circuit and active voltage adjustable current mirror are analyzed. The analysis is based on the modified Ebers–Moll equations [7] to include the Early effect and the low-current β degradation effect, given by

$$I_C = (1 + V_{CE}/V_A) I_S e^{V_{BE}/V_T} \quad (1)$$

and

$$I_B = \frac{I_S}{B_F} e^{V_{BE}/V_T} + I_{SE} e^{V_{BE}/N_E V_T} \quad (2)$$

where

- B_F maximum forward current gain;
- I_S $qA\overline{D}_n n_i^2/Q_B$;
- A cross sectional area of the emitter;
- Q_B number of doping atoms in the base per unit area of the emitter;
- $\overline{D}_n$ average effective value of the electron diffusion constant in the base;
- V_A forward Early voltage;
- I_{SE} base-emitter leakage saturation current;
- N_E base-emitter leakage emission coefficient;
- V_T kT/q.

The current gain β of the transistor is defined as

$$\beta = \frac{I_C}{I_B}. \quad (3)$$

Using (1)–(3) gives

$$\beta(V_{CE}, I_C) = \frac{B_F(1 + V_{CE}/V_A)^{1/N_E}}{(1 + V_{CE}/V_A)^{([1/N_E]-1)} + B_F I_S^{-1/N_E} I_{SE} I_C^{([1/N_E]-1)}}. \quad (4)$$

For $V_A \gg V_{CE}$, (4) can be simplified to

$$\beta(I_C) = \frac{B_F}{1 + B_F I_S^{-1/N_E} I_{SE} I_C^{([1/N_E]-1)}}. \quad (5)$$

It can readily be shown that the current gain of the cascoded current mirror without β degradation effect cancellation [Fig. 2(d)] is given by

$$G_{\text{mirr}}(I_{\text{in}}) = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{HH'(1+\epsilon)}{1 + (HH'(1+\epsilon)+1)/\beta(HI_{\text{in}})} \quad (6)$$

where

$$H = \frac{I_{S2}}{I_{S1}} e^{V_{\text{CTRL}}/V_T} \quad (7)$$

$$V_{\text{CTRL}} = I_{\text{CTRL}} R_b - I_{\text{CONST}} R_b \quad (8)$$

$$H' \approx 1 - \frac{V_T \ln(I_{S3} I_{S2}/I_{S4} I_{S1}) + V_{\text{CTRL}}}{V_A} \quad (9)$$

$$\epsilon \approx e^{(I_{\text{in}}(R_{\text{eq1}} - HR_{\text{eq2}}))/V_T} - 1 \quad (10)$$

$$R_{\text{eq1}} = R_{E1} + R_b/(1 + \beta(I_{\text{in}})) \quad (11)$$

$$R_{\text{eq2}} = R_{E2} + R_b/(1 + \beta(HI_{\text{in}})) \quad (12)$$

$$R_{E1} = r_{e1} + r_{b1}/(1 + \beta(I_{\text{in}})) \quad (13)$$

$$R_{E2} = r_{e2} + r_{b2}/(1 + \beta(HI_{\text{in}})) \quad (14)$$

r_{ei} = emitter bulk resistance of Q_i
r_{bi} = base bulk resistance of Q_i.

The Early effect is responsible for H', which is fairly close to unity. The errors due to the parasitic resistances and internal resistance of the voltage source are represented by the factor ϵ. At low-level signal currents, the value of ϵ is close to zero and does not affect the linearity but for high-level signal currents this is responsible for the nonlinearity. Since current gain depends on β, the β degradation effect introduces nonlinearity at low signal current levels.

The current gain of the current mirror shown in Fig. 2(f) is given by

$$G_{\text{mirr}}(I_{\text{in}}) = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1 + 1/\beta(I_{\text{in}})}{1 + 1/\beta(HI_{\text{in}})} HH'(1+\epsilon). \quad (15)$$

In (15), H' and ϵ are given by (9) and (10), respectively. The nonlinearity due to β degradation effect is very small in this case because of the cancellation of $\beta(I_{\text{in}})$ with $\beta(HI_{\text{in}})$.

The current gain of the current mirror shown in Fig. 3(b) is also given by (15), with modified H and R_b as

$$H \approx \frac{I_{S2} I_{Sa}}{I_{S1} I_{Sb}} \frac{(I_{\text{CTRL}})}{(I_{\text{CONST}} - I_{\text{CTRL}})} \quad (16)$$

$$R_b \approx \frac{1}{r_{ob} g_{mb} g_{me}}. \quad (17)$$

It should be noted that the current gain of the active voltage source ACM is, to first order, independent of temperature.

IV. Integrated Circuit Implementation

The circuits were implemented in a commercial 0.8-μm BiCMOS process, fabricated through the Canadian Microelectronics Corporation. The base resistor ACM and active voltage source ACM were fabricated on separate IC's and internal connections were taken out to package pins to test the current mirror with and without a β degradation immune cascode circuit. The plot of the layout of the IBACYCM1 IC, which is the implementation of the base resistor ACM shown in Fig. 2(f),[1] is shown in Fig. 4. The die area excluding bonding pads and logo is 156 μm × 210 μm. The plot of the layout of the IBACYCM2 IC, which is the implementation of the active voltage source ACM shown in Fig. 3(b), is shown in Fig. 5. The die area excluding bonding pads and logo is 175 μm × 270 μm. The positive power supply V_{DD} and negative power supply V_{EE} were chosen to be 3.5 V and −1.5 V, respectively, because the maximum power supply was limited to 5 V by the process. In the case of a single power supply, a 1.5 V potential drop between *Ground* and V_{EE} can be achieved by using two diode-connected transistors connected in series with a current source.

V. Analytical, Simulation, and Test Results

The current mirrors were designed for signal currents ranging from 50 pA to 0.2 mA. The maximum output current was limited to 0.2 mA.

[1] The internal connections were taken out to package pins in such a way that the base resistor ACM shown in Fig. 2(d) could also be tested.

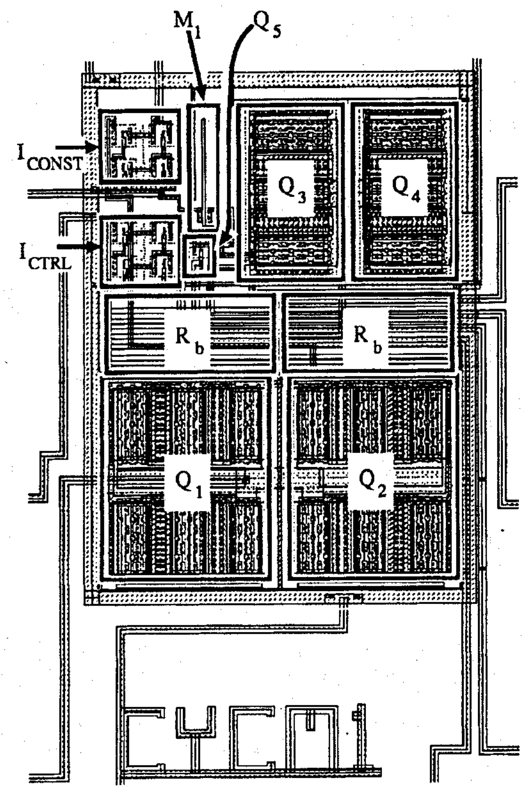

Fig. 4. Layout of the IBACYCM1 IC.

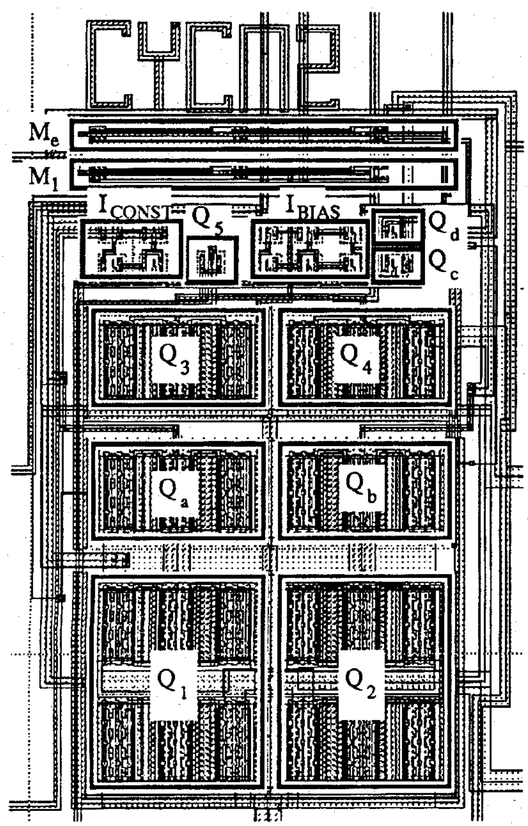

Fig. 5. Layout of the IBACYCM2 IC.

The β degradation effect is severe at low signal currents. To study the performance of the circuit, percent normalized

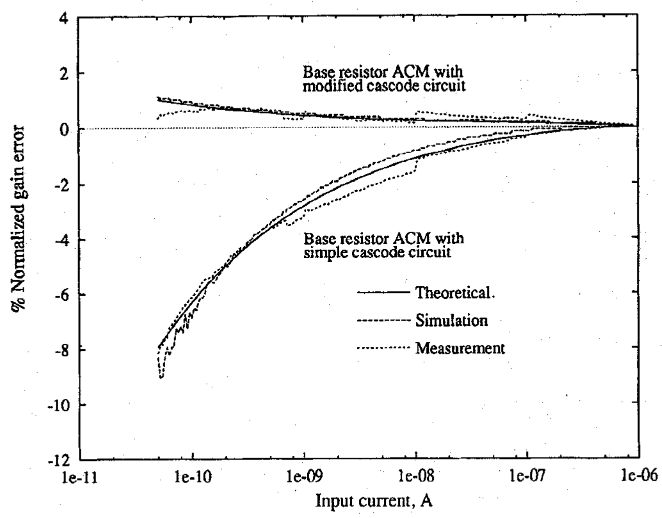

Fig. 6. Nonlinearity due to β degradation effect at a nominal gain of 16.

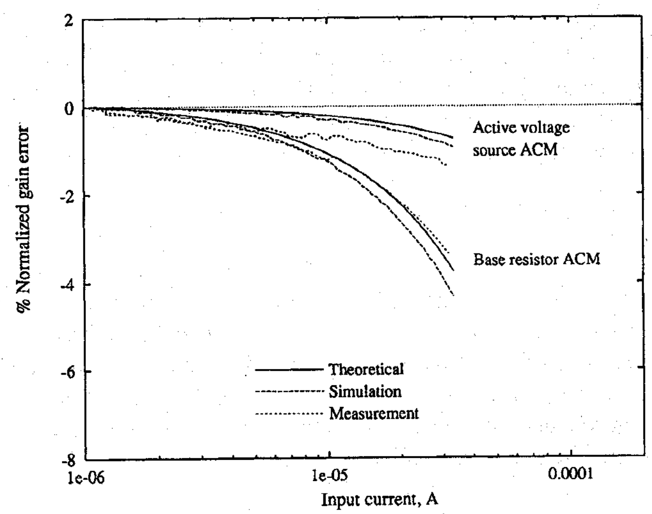

Fig. 7. Nonlinearity due to internal resistance of voltage source and parasitic resistances at a nominal gain of 16.

gain errors defined as $100 \times (G_{\mathrm{mirr}} - G_{\mathrm{mirr}_o})/G_{\mathrm{mirr}_o}$ are plotted where G_{mirr_o} is the current gain when the input current is equal to 1 μA. Fig. 6 shows the percent normalized gain errors of the base resistor current mirrors with [Fig. 2(f)] and without [Fig. 2(d)] the β degradation immune cascode circuit at a nominal current gain (H) of 16. It is evident that by using the β degradation immune cascode circuit, the nonlinearity is decreased by approximately one order of magnitude.

At high signal currents, the parasitic resistances and voltage source internal resistance start introducing gain error. Fig. 7 shows the percent normalized gain errors of the base resistor ACM [Fig. 2(f)] and the active voltage source ACM [Fig. 3(b)] at a nominal current gain of 16. The linearity improves by using an active voltage source.

Fig. 8 shows the input current versus output current characteristics of the base resistor [Fig. 2(f)] and the active voltage source ACM [Fig. 3(b)]. Fig. 9 shows the current gains of the base resistor ACM and the active voltage source ACM at control signal levels such that the gains are approximately 0.25, 1, 4, and 16. The maximum current gain of the ACM

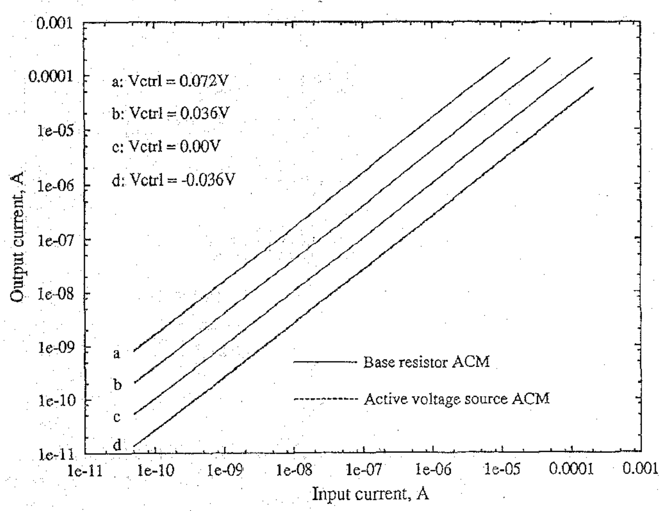

Fig. 8. Measured input–output characteristics of the ACM's.

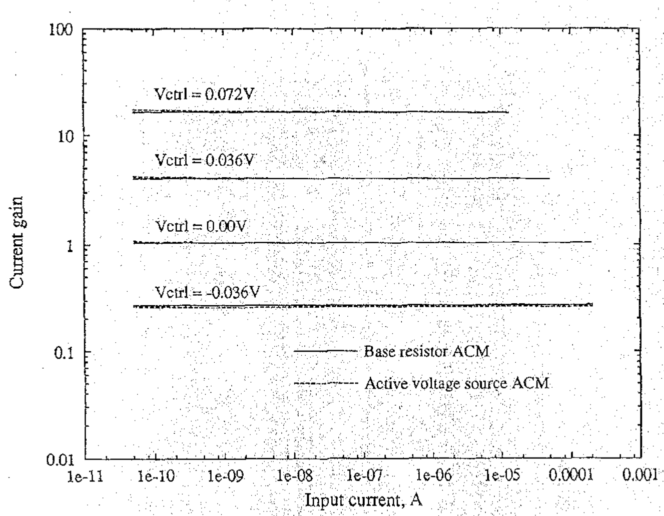

Fig. 9. Measured current gain of the ACM's.

with simple cascode circuit is limited to the current gain, β, of the transistor. The maximum current gain is increased in the β degradation immune cascode current mirrors. In circuits where small gain variation is needed, the BiCMOS current mirrors can be very useful because of their large dynamic range of more than 120 dB.

VI. Conclusion

Two novel adjustable gain current mirrors with high output resistance and improved linearity have been described. An analysis based on a bipolar transistor model that includes the Early effect has been presented and the results have been verified by SPICE simulation and experiment using a commercial 0.8-μm BiCMOS process.

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