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Analysis and Design of HBT Cherry–Hooper Amplifiers With Emitter-Follower Feedback for Optical Communications

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Abstract—In this article, the large-signal, small-signal, and noise performance of the Cherry–Hooper amplifier with emitter-follower feedback are analyzed from a design perspective. A method for choosing the component values to obtain a low group delay distortion or Bessel transfer function is given. The design theory is illustrated with an implementation of the circuit in a 47-GHz SiGe process. The amplifier has 19.7-dB gain, 13.7-GHz bandwidth, and ± 10 -ps group delay distortion. The amplifier core consumes 34 mW from a -3.3 -V supply.

Index Terms—Bessel response, Cherry–Hooper, emitter-follower feedback, optical communications, SiGe HBT.

I. INTRODUCTION

THE CHERRY–HOOPER amplifier with emitter-follower feedback (CHEF), shown in Fig. 1, is widely used in limiting amplifiers and decision circuits in fiber-optic receivers [1]–[4]. The use of these amplifiers operating at 40 Gb/s in InP technology has recently been demonstrated [5], [6]. The amplifier shown includes resistor R_2 , an addition suggested by Greshishchev and Schvan in order to raise the gain [7]. Although this circuit is useful as a high-performance broadband amplifier, it can have excessive gain and group delay peaking for certain choices of the component values. Designing the gain to peak with frequency may give the highest bandwidth, but this results in the group delay peaking with frequency as well and leads to a distorted eye pattern [4]. For this reason, it is necessary to strike a balance between gain and delay flatness and bandwidth in transceiver amplifiers.

Ohhata *et al.* presented an analysis of the CHEF amplifier for an implementation using selective-epitaxial SiGe HBTs for which the parasitic capacitances are relatively small and the base resistance is relatively large. In that work, the base resistance of the small feature size HBTs had a significant effect on the small-signal transfer function of the amplifier. In this work, we examine amplifiers that are designed with SiGe HBTs having base resistances less than 100Ω [8]. To our knowledge, the small-signal behavior of the CHEF amplifier using such devices and using R_2 has not been characterized in a way that would allow designers to optimize group delay and bandwidth. In this

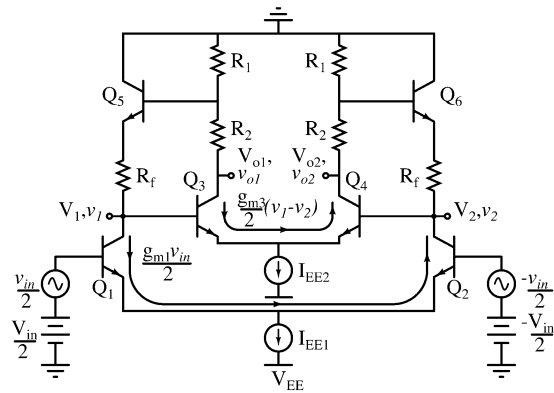


Fig. 1. Cherry–Hooper amplifier with emitter-follower feedback.

paper, equations for the frequency response, dc transfer characteristic, and output noise of the amplifier are given and are used to develop design guidelines. Using these guidelines, the amplifier may be designed as a second-order all-pole system to have a Bessel transfer function.

This paper is arranged as follows. In Section II, the large-signal performance of the amplifier is considered. In Section III, a small-signal high-frequency model of the amplifier is presented. Suggestions for low-noise design are given in Section IV. Section V uses the equations that are presented to design a 13.7-GHz bandwidth, 19.7-dB gain implementation of the amplifier in a 47-GHz f_t SiGe HBT technology. Measurement results are presented to confirm the theory.

II. LARGE-SIGNAL PERFORMANCE

The large-signal performance of the amplifier may be understood by first considering the dc transfer characteristic. In Fig. 1, uppercase variables are used to represent dc voltages and currents. In Appendix I, (1) and (2) are derived for the amplifier in Fig. 1.

$$\begin{aligned}
 V_1 - V_2 \cong & R_1 I_{EE2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right) \\
 & + R_f I_{EE1} \cdot \tanh\left(\frac{-V_{in}}{2V_T}\right) \\
 & + V_T \cdot \ln\left(\frac{I_{EE1}}{1 + e^{V_{in}/V_T}} + \frac{I_{EE2}}{\beta_{DC}(1 + e^{(V_1 - V_2)/V_T})}\right) \\
 & - V_T \cdot \ln\left(\frac{I_{EE1}}{1 + e^{-V_{in}/V_T}} + \frac{I_{EE2}}{\beta_{DC}(1 + e^{(V_2 - V_1)/V_T})}\right)
 \end{aligned} \tag{1}$$

$$V_{o1} - V_{o2} \cong (R_1 + R_2) I_{EE2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right). \tag{2}$$

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In these equations, β_{DC} is the dc common emitter current gain of the transistors and V_T is the thermal voltage of approximately 26 mV at room temperature. These expressions show that the dc voltage difference $V_1 - V_2$ for a given V_{in} may be calculated through iteration, and then $V_{o1} - V_{o2}$ may be calculated.

A first observation from (1) and (2) is that R_2 will only scale the output voltage, without affecting its basic shape. Hence, increasing R_2 is an effective means of increasing the output voltage swing of the amplifier. However, (2) also shows that in order for $V_{o1} - V_{o2}$ to reach the maximum output swing of $(R_1 + R_2)I_{EE2}$, \tanh must reach its full value of ± 1 . This occurs when $|V_1 - V_2| \gg V_T$. Having $V_{o1} - V_{o2}$ reach its approximate full output swing is desirable in the presence of large high-frequency signals, because the resulting voltage will then be $\pm(R_1 + R_2)I_{EE2}$, which is known and well defined. In contrast, the voltage $V_1 - V_2$ will not be well defined, since it depends on the emitter voltages of Q_5 and Q_6 , which will suffer from amplitude overshoot due to capacitive feedthrough at the emitters of Q_5 and Q_6 .

As a further consideration, I_{EE1} and I_{EE2} should be large enough to achieve a high f_t for the HBTs in the amplifier. However, there is a range of bias current for certain SiGe HBT technologies where the current may be changed, for example by a factor of two, without significantly affecting f_t [9]. This gives the designer the freedom to choose the bias currents at or somewhat lower than that required for peak f_t , and near peak f_t may still be achieved.

III. SMALL-SIGNAL ANALYSIS

Fig. 2 shows the small-signal differential-mode half circuit of the amplifier with only the dominant parasitics. It is assumed that the circuit is symmetrical, so that the small-signal parameters of Q_1 and Q_2 , for example, are equal. In the following analysis, the base-emitter capacitance of transistor k will be denoted as $C_{\pi k}$, the base-collector capacitance as $C_{\mu k}$, and the collector-substrate capacitance as C_{subk} . Capacitance C_1 represents the sum of C_{sub1} , and $C_{\mu 1}$ and $C_{\mu 3}$ reflected to node v_1 using Miller's theorem. The fact that $C_{\pi 3}$ connects to ground through r_{e3} will be neglected and $C_{\pi 3}$ will simply be added to C_1 . Specifically

$$C_1 = C_{\pi 3} + \left(1 - \frac{1}{A_1}\right) C_{\mu 1} + C_{sub1} + C_{\mu 3}(1 - A_2) \quad (3)$$

where A_1 and A_2 are the gains across $C_{\mu 1}$ and $C_{\mu 3}$, respectively, and are given by

$$A_1 \cong -\frac{r'_{d3}(R'_f + r_{d5})}{r'_{d1}(r'_{d3} + R_1)} \quad (4)$$

$$A_2 \cong -\frac{R_1 + R_2}{r'_{d3}} \quad (5)$$

where $r_{dk} = 1/g_{mk}$, $r'_{dk} = 1/g_{mk} + r_{ek}$, g_{mk} is the transconductance of transistor k , r_{ek} is the parasitic emitter resistance of transistor k , and $R'_f = R_f + r_{e5}$. The component of $C_{\mu 1}$ reflected to the base of Q_1 through Miller effect has been ignored, since the gain across Q_1 is usually small and so the Miller capacitance will be much less than $C_{\pi 1}$. Also in Fig. 2, the base-emitter resistance $r_{\pi k}$ for a transistor k has been rewritten

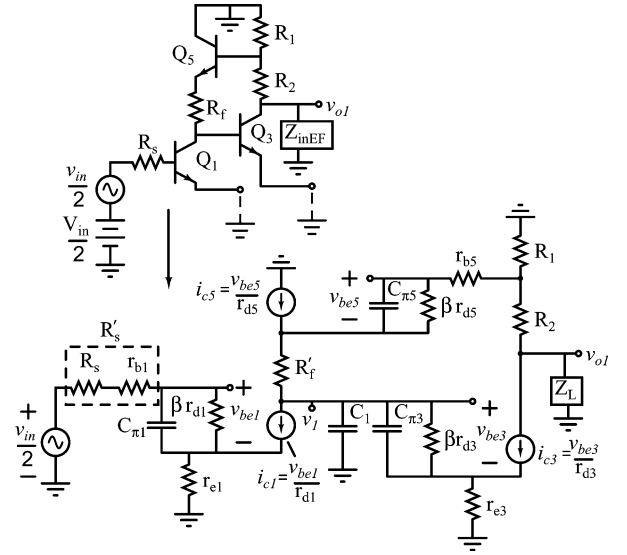


Fig. 2. Amplifier small-signal differential-mode half circuit including source and load impedances.

using the well-known identity $r_{\pi k} \cong \beta r_{dk}$, where β is the low-frequency ac common emitter current gain. These approximations facilitate analysis without introducing significant error, as will be shown.

The small-signal transfer function may be broken into two parts, $v_{o1}/v_{in} = v_{be1}/v_{in} \times v_{o1}/v_{be1}$. The transfer function v_{be1}/v_{in} is calculated to be

$$\frac{v_{be1}}{v_{in}} \cong \frac{r_{d1}}{2\{r'_{d1} + r_{d1}sC_{\pi 1}(R'_s + r_{e1})\}} \quad (6)$$

This expression has a single pole resulting from $C_{\pi 1}$ and mainly from R'_s , which is the resistance of the input signal source plus the base resistance of the input HBT. In practice, the amplifier is usually driven by an emitter-follower, which has a very low output impedance, making R'_s small. As a result, this pole will be at a frequency significantly higher than the bandwidth of the overall amplifier.

The stage following the amplifier is usually an emitter-follower output buffer, and the amplifier is loaded by the input impedance of this emitter-follower, Z_{inEF} . This impedance, along with C_{sub3} and the Miller capacitance of $C_{\mu 3}$ reflected to node V_{o1} , form the load impedance Z_L , according to

$$\frac{1}{Z_L} = \frac{1}{Z_{inEF}} + sC_{sub3} + sC_{\mu 3} \left(1 - \frac{1}{A_2}\right). \quad (7)$$

The magnitude of the impedance Z_{inEF} decreases with frequency, and so Z_L may be modeled to first order by a capacitor C_L . A more accurate prediction of the amplifier response may be obtained with a more detailed formulation of Z_{inEF} , as described in Appendix II.

Nodal analysis was used to find the transfer function v_{o1}/v_{be1} , which is derived in Appendix III. With the assumption that $Z_L \cong 1/C_L$, v_{o1}/v_{be1} may be approximately expressed as

$$\frac{v_{o1}}{v_{be1}} \cong \frac{1}{r_{d1}r'_{d3}C_1C_L \left[s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right]} \quad (8)$$

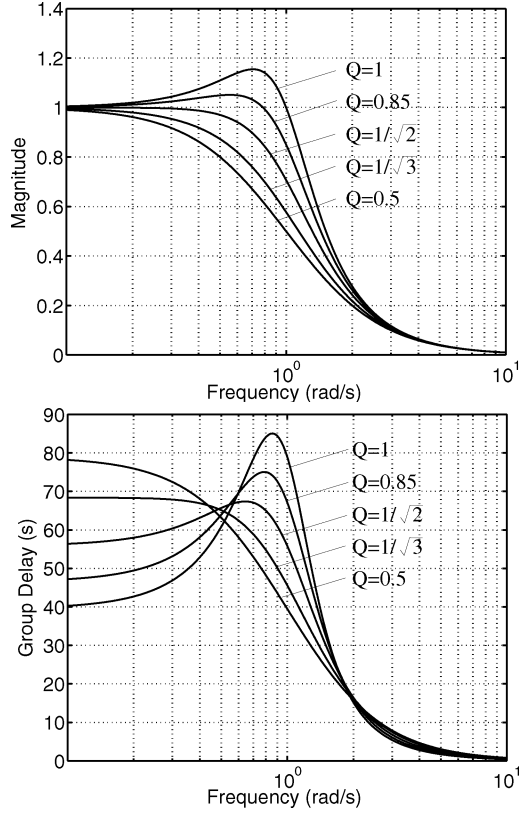


Fig. 3. Magnitude and group delay responses for a second-order system.

where Q and ω_o are the pole quality factor and pole frequency given by

$$Q = \left[\frac{C_1 C_L (R_1 + R_2) (R'_f + r_{d5}) (R_1 + r'_{d3})}{r'_{d3} \{C_1 (R'_f + r_{d5}) + C_L (R_1 + R_2)\}^2} \right]^{1/2} \quad (9)$$

$$\omega_o = \left[\frac{R_1 + r'_{d3}}{r'_{d3} C_1 C_L (R_1 + R_2) (R'_f + r_{d5})} \right]^{1/2}. \quad (10)$$

Equations (9) and (10) are valid for $R'_f/R_1 > 2$. The latter equation indicates that the pole frequency ω_o , which is one indication of amplifier bandwidth, is inversely proportional to the square root of C_1 , C_L , and R'_f if $R'_f \gg r_{d5}$. This indicates that although increasing R'_f raises the amplifier gain, it decreases the bandwidth. Equation (9) may be further simplified if $C_1 (R'_f + r_{d5}) \gg C_L (R_1 + R_2)$ to

$$Q \cong \left[\frac{C_L (R_1 + R_2) (R_1 + r'_{d3})}{r'_{d3} C_1 (R'_f + r_{d5})} \right]^{1/2}. \quad (11)$$

This shows that increasing R_1 raises Q , and increasing R'_f or C_1 lowers Q . Furthermore, increasing R_2 will result in modest increases in Q , and a comparable decrease in ω_o , two effects which may be expected to leave the bandwidth roughly unchanged. This is consistent with the observation of Greshishchev and Schvan, who noted that increasing R_2 in the range $0 < R_2/R_1 < 2.5$ had little effect on the bandwidth but increased the gain significantly [7].

The two poles in (8) located at ω_o are a complex conjugate pair for $Q > 0.5$ and they dominate the frequency response

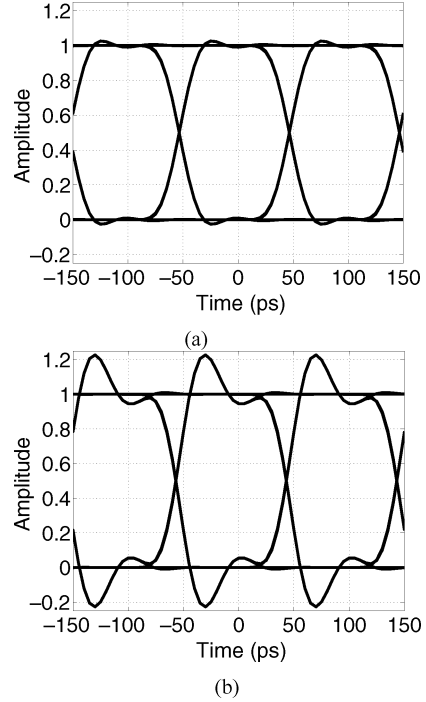


Fig. 4. Eye diagrams for a 10-Gb/s signal filtered with second-order systems having (a) $Q = 1/\sqrt{3}$ and (b) $Q = 1.0$.

of the CHEF amplifier. Fig. 3 shows the magnitude and group delay responses for such a system for different values of Q and for $\omega_o = 1$ rad/s. The case where $Q = 1/\sqrt{2} \cong 0.707$ corresponds to a second-order Butterworth response, where the magnitude response is maximally flat. The case where $Q = 1/\sqrt{3} \cong 0.58$ corresponds to a second-order Bessel response, where the group delay is maximally flat [10]. Fig. 4 shows eye diagrams of 10-Gb/s signals which have passed through second-order systems with Q values of $1/\sqrt{3}$ and 1.0, respectively, and with $\omega_o = 2\pi \cdot 15 \times 10^9$ rad/s. The eye diagram for the system with $Q = 1.0$ is distorted due to the gain peaking and group delay distortion of that system. To avoid this type of distortion, it is always desirable to have a Q factor of approximately $1/\sqrt{3}$ for broadband optical applications. The disadvantage of such a design is that it has less bandwidth than a design with a higher Q factor.

A. Design Example

The method in which the amplifier may be designed to have $Q = 1/\sqrt{3}$ can be illustrated through an example. Bias currents are first chosen based, for instance, on the desired amount of power dissipation. The value of I_{EE2} will also partially determine the output voltage swing. For the purpose of illustration, one amplifier with two different current bias levels will be considered here. One bias level is $I_{EE1} = I_{EE2} = 1.0$ mA, and the other bias level is $I_{EE1} = 3.0$ mA and $I_{EE2} = 3.2$ mA, chosen based on output swing. Higher currents than these may cause a biasing problem when a 3.3-V or lower supply voltage is used.

When designing the amplifier, the emitter length L_E of the HBTs should be chosen to provide peak or near peak f_t , assuming that such an L_E is large enough to safely handle the desired amount of bias current. The emitter length of Q_1 and Q_2

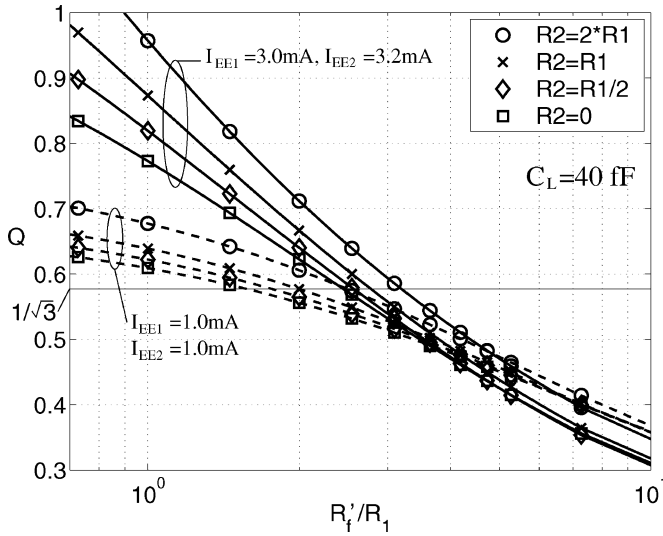


Fig. 5. Plot of Q factor for different values of R_1 , R_2 , and R'_f .

in the first stage of a limiting amplifier chain should be chosen based on noise considerations as well, as will be shown in Section IV. For the present circuit, dual stripe emitters are used for all transistors, each emitter stripe width is $0.5 \mu\text{m}$, and the emitter length of each stripe is $5.0 \mu\text{m}$ for Q_1 , Q_2 , Q_5 , and Q_6 , and $2.5 \mu\text{m}$ for Q_3 and Q_4 . Once the bias currents and L_E of the HBTs are chosen, the only unknowns in (8) are R_1 , R_2 , R'_f , and Z_L . Z_L may be calculated by (7) with a capacitance chosen to model Z_{inEF} . The choice of the resistors R_1 , R_2 , and R'_f will determine the gain and bandwidth of the amplifier, and the Q factor of the two dominant poles. R_1 may be chosen based on the desired amount of output swing, and is chosen as 55Ω for this example. The values of R'_f and R_2 may then be varied in order to observe the obtainable performance. Figs. 5–7 show plots of Q , 3-dB bandwidth, and low-frequency gain, respectively, versus R'_f/R_1 for different values of R_2 . At the lower current bias level, the circuit has reduced bandwidth because the f_t of the HBTs is reduced to 50%-75% of the peak value. These plots were generated using the complete expression for v_{o1}/v_{be1} in Appendix III, (20), with $Z_L = 1/(sC_L)$ and $C_L = 40 \text{ fF}$. Of this capacitance, approximately 15 fF represents $C_{\mu3}$ reflected to node v_{o1} and $C_{\text{sub}3}$, and 25 fF was used to model Z_{inEF} .

Using these plots, consider the amplifier when biased with $I_{EE1} = 3.0 \text{ mA}$ and $I_{EE2} = 3.2 \text{ mA}$. From Fig. 5, it is seen that in order to have $Q \cong 1/\sqrt{3}$, R'_f/R_1 should be in the range from 2.3 to 2.7. This shows that the ratio R'_f/R_1 is highly constrained for a fixed set of bias currents. For this example, $R_f = 160 \Omega$ gives $R_f/R_1 = 2.9$. This gives a Q factor slightly lower than $1/\sqrt{3}$ and will allow for some variation in the load impedance Z_L without introducing significant group delay peaking. From Figs. 6 and 7, it may be seen that for $R'_f/R_1 \cong 2.9$ the bandwidth ranges from 11.5 to 14.5 GHz and the gain ranges from 14.4 to 24.0 dB for different values of R_2 . Choosing $R_2 = R_1 = 55 \Omega$ gives a reasonable compromise, leading to a theoretical bandwidth of 12.9 GHz and a gain of 20.5 dB.

It should be noted that I_{EE1} and I_{EE2} need not be equal. However, with L_E of Q_1 and Q_2 chosen to be $5 \mu\text{m}$ to lower

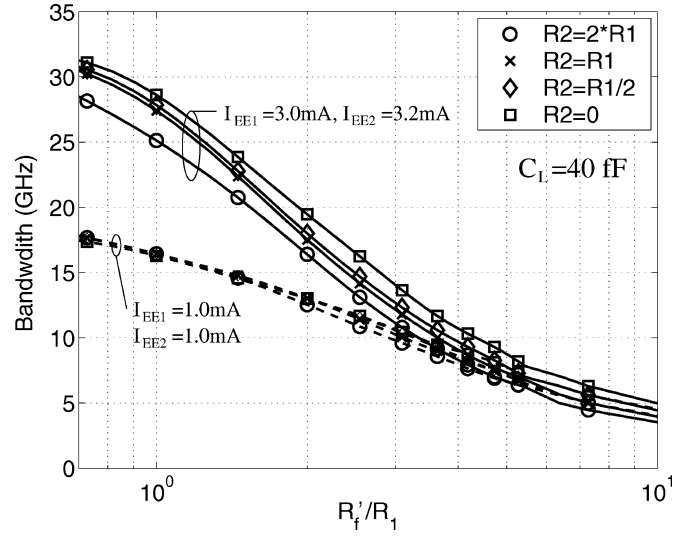


Fig. 6. Plot of 3-dB bandwidth for different values of R_1 , R_2 , and R'_f .

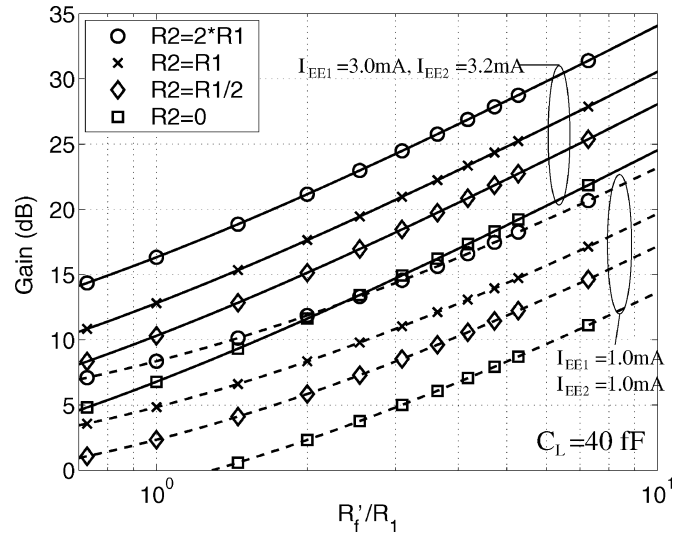


Fig. 7. Plot of low-frequency gain for different values of R_1 , R_2 , and R'_f .

r_b , I_{EE1} must be 3.0 mA to obtain near peak f_t . With $I_{EE2} = 3.2 \text{ mA}$ chosen to obtain the desired output swing and peak f_t , the currents end up being nearly equal.

IV. AMPLIFIER NOISE PERFORMANCE

The CHEF amplifier often follows the transimpedance amplifier (TIA) in a fiber optic receiver. Hence, in addition to having a good frequency response, low-noise operation is desired in the first amplifier following the TIA. In this section, a simple expression is given for the output noise power spectral density (PSD) of the amplifier.

In the following analysis, the mean square thermal noise voltage due to a given resistor R will be expressed as $\overline{e_R^2}$, where $\overline{e_R^2} = 4kTR\Delta f$ and where k is Boltzmann's constant, T is temperature in Kelvin, and Δf is equivalent noise bandwidth. For a dc collector current I_C , the mean square collector shot noise current will be expressed as $\overline{i_{ck}^2}$ for the k th transistor, where $\overline{i_{ck}^2} = 2qI_{Ck}\Delta f$ and where q is the electron charge.

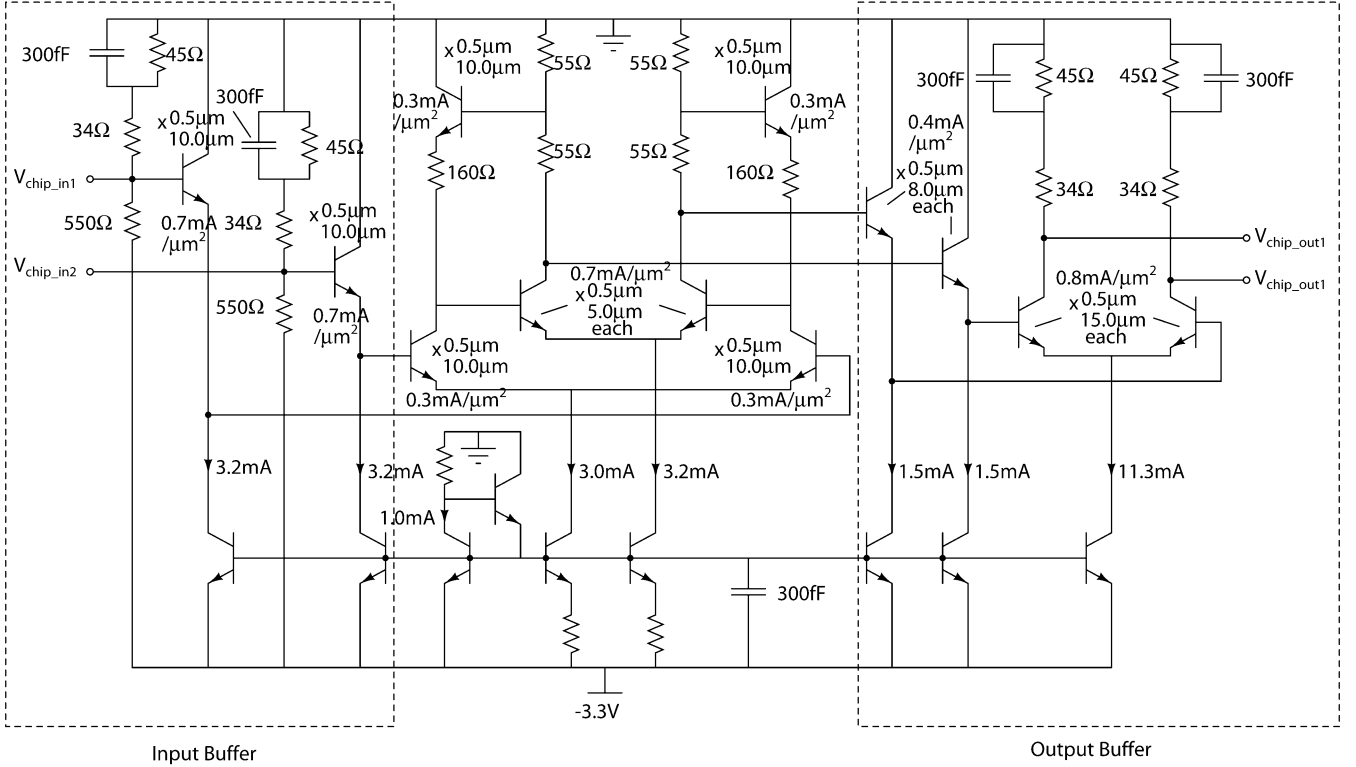


Fig. 8. Schematic diagram of amplifier test circuit.

Using the above notation, an example calculation of the differential output noise due to i_{c1}^2 is given in Appendix IV. In the same way, the differential noise PSD between $v_{o1}(t)$ and $v_{o2}(t)$ due to all noise sources in the amplifier is calculated as

$$\frac{\overline{v_o^2}}{\Delta f} \cong \frac{2(R_1 + R_2)^2}{(R_1 + r'_{d3})^2} \left[\frac{e_{R_f}^2}{\Delta f} + \frac{(R'_f + r_{d5})^2}{r_{d1}^2} \times \left(\frac{e_{r_{b1,2}}^2}{\Delta f} + \frac{e_{r_{e1,2}}^2}{\Delta f} + r_{d1}^2 \frac{i_{c1,2}^2}{\Delta f} \right) \right] \quad (12)$$

where, for example, $\overline{e_{r_{b1,2}}^2}$ is the noise of either r_{b1} or r_{b2} . The input referred differential noise PSD may be obtained if desired by dividing this equation by the square of the low frequency differential amplifier gain, given by the product of (4) and (5). From (12), it is seen that if $(R'_f + r_{d5})^2 / r_{d1}^2 \gg 1$ and $r_{b1} \gg r_{e1}$, then the most important amplifier noise sources will be the collector current shot noise and base resistance thermal noise of Q_1 or Q_2 , $i_{c1,2}^2$ and $e_{r_{b1,2}}^2$, respectively. As an example, consider the amplifier with $I_{EE1} = 3.0$ mA, $I_{EE2} = 3.2$ mA, $R_1 = R_2 = 55 \Omega$, and $R_f = 160 \Omega$. Table I gives the values predicted by the terms in (12) with the values simulated at 1 GHz using 47-GHz f_t SiGe HBTs. In Table I, it is clear that the parasitic base resistance and collector shot noise of $Q_{1,2}$ are the dominant noise sources. The collector current shot noise of $Q_{1,2}$ is difficult to reduce, since a certain amount of current is required for high f_t and gain. However, the base resistance may be minimized by increasing the emitter length at a fixed emitter width while keeping the bias current constant. The effective emitter length may also be increased by using multiple

 TABLE I
 DIFFERENTIAL OUTPUT NOISE OF THE AMPLIFIER AT 1 GHz

Noise Source	Simulated Noise ($V^2/Hz \times 10^{-17}$)	Simulated % of Total	Calculated Noise ($V^2/Hz \times 10^{-17}$)	% Error
$Q_{1,2} : r_b$	13.6	65.1%	15.4	13.2%
$Q_{1,2} : I_c$	3.83	18.3%	4.11	7.3%
$Q_{1,2} : r_e$	1.23	5.9%	1.39	13.0%
$R_f \times 2$	0.89	4.3%	1.01	13.5%
Totals	19.6	93.6%	21.9	11.7%

transistors in parallel. This will result in some decrease in f_t , but a greater decrease in noise than in bandwidth. Using multiple transistors also reduces self heating in these HBTs [7].

V. EXPERIMENTAL RESULTS

The design described in Section III-A was fabricated in a 47-GHz f_t SiGe process. The schematic diagram of the amplifier is shown in Fig. 8. The input of the circuit is an emitter-follower input buffer, with resistors and a capacitor arranged to maintain an impedance match up to 10 GHz when the input leads are wire bonded. It was found that if a simple 50- Ω resistor was used, the parasitic capacitance at the input node of the HBTs and approximately 1 nH of bondwire inductance would unacceptably degrade the input match if the chip was wire bonded, as is typically required for packaging. By having the approximate 70- Ω input impedance at low frequencies, it was found that the effects of the 300-fF capacitor and the bondwire inductance combine to achieve a better 50- Ω match above 5 GHz [7].

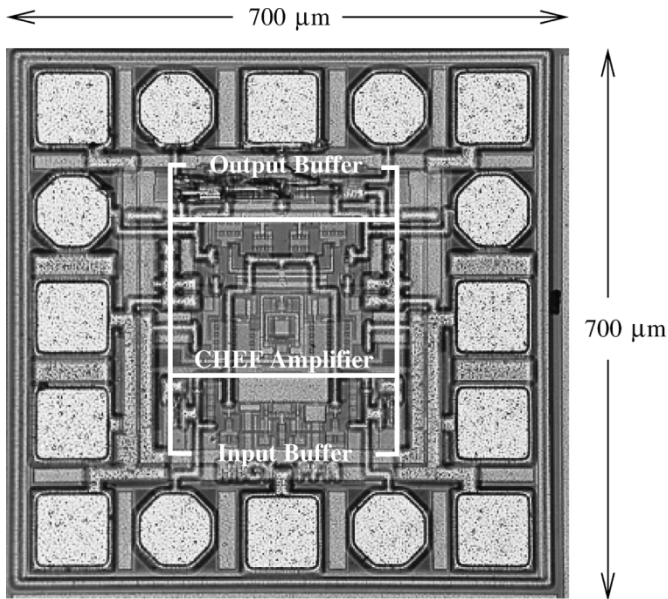


Fig. 9. Integrated circuit microphotograph.

However, for the measurements presented in this section, wafer probing was used to provide a characterization of the amplifier that is unobscured by bondwire parasitics.

The output buffer is a differential pair with an impedance match similar to that used in the input buffer. The important component values of the amplifier are shown in the schematic diagram. The amplifier core draws 10.2 mA from a -3.3-V supply. A microphotograph of the integrated circuit is shown in Fig. 9.

Fig. 10 shows the theoretical transfer function of the amplifier predicted by (6) and (20), the simulated transfer function with and without resistive and capacitive layout parasitics, and the deembedded measured transfer function. The measured gain was deembedded from a measurement of S_{21} taken with a -20-dBm input signal. For the theoretical transfer function calculation, the load impedance was modeled using (7) and (18). All of the simulated curves in this section were generated using Cadence Spectre software. The error between the theoretical and deembedded measurement is less than 1.2 dB between 0–5 GHz, and is less than 0.8 dB between 5–15 GHz. In the layout, multiple resistors in parallel were used to implement R_1 and R_2 , leading to increased metallization area connecting to these resistors. The difference in the simulated response with parasitics is partially attributed to the capacitance of this metallization to the substrate and to surrounding nodes.

Fig. 11 shows a comparison of the theoretical group delay, the simulated group delay with and without resistive and capacitive layout parasitics, and the measured group delay. The group delay distortion up to 10 GHz is approximately $\pm 10\text{-ps}$ theoretical, $\pm 6\text{-ps}$ simulated without layout parasitics, $\pm 12\text{-ps}$ simulated with layout parasitics, and $\pm 10\text{-ps}$ measured. In this case, the theory provides a reasonable prediction of group delay for design purposes.

The noise figure (NF) was measured at one output terminal with the signal applied to one input terminal, and the other input and output terminals were terminated in $50\ \Omega$. The measured NF

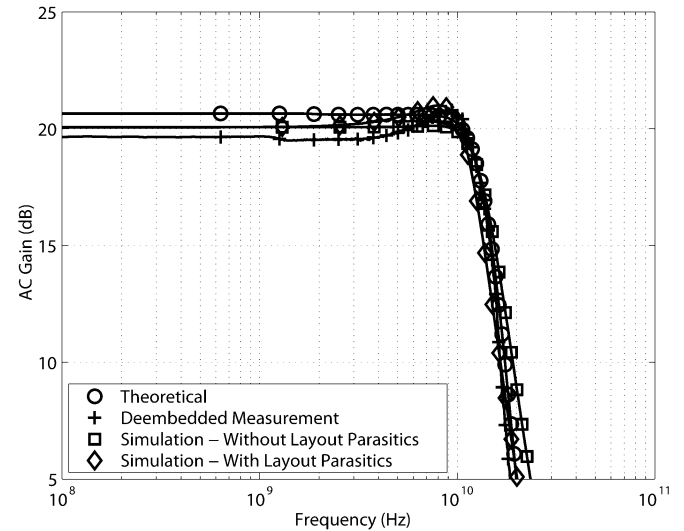


Fig. 10. Comparison of theoretical gain based on (6) and (20), simulated gain, and measured gain.

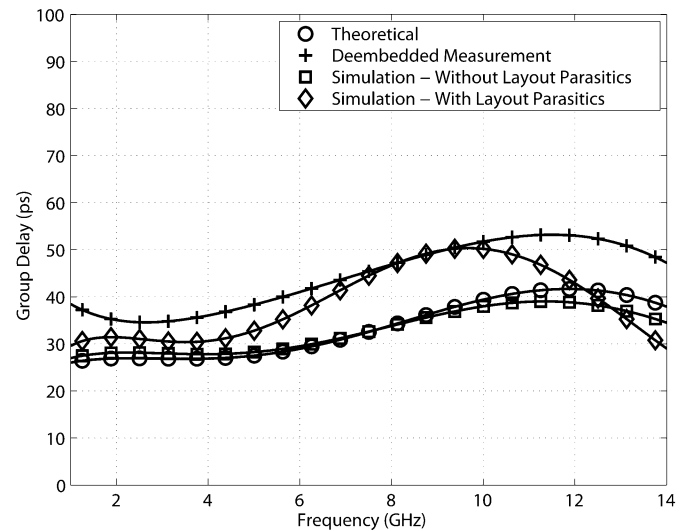


Fig. 11. Comparison of theoretical group delay based on (6) and (20), as well as simulated and measured group delay.

is 14.7 dB at 1 GHz. The equivalent de-embedded differential noise at the output of the amplifier core is $2.36 \times 10^{-16} \text{ V}^2/\text{Hz}$. Comparing this with the theoretical output noise from Table I, it is observed that (12) predicts the measured noise with -8% error.

Fig. 12 shows measured eye diagrams for a data rate of 10 Gb/s. A PRBS signal with a pattern length of $2^{31} - 1$ was used for all measurements. Fig. 12(a) shows the signal at the output of the pattern generator, and Fig. 12(b)–(d) shows the single-ended amplifier output eye for a differential input signal with amplitudes of 7, 20, and 400 mV_{pp}, respectively. The data eye has good opening and low overshoot for all cases. In order to have a more square eye, which is desirable, the required bandwidth is approximately 1.5 times the clock rate, or 15 GHz for 10 Gb/s. Although the bandwidth of the amplifier is 13.7 GHz, the inclusion of the input and output buffers reduces the bandwidth to 11.2 GHz. A bandwidth of 15 GHz could be

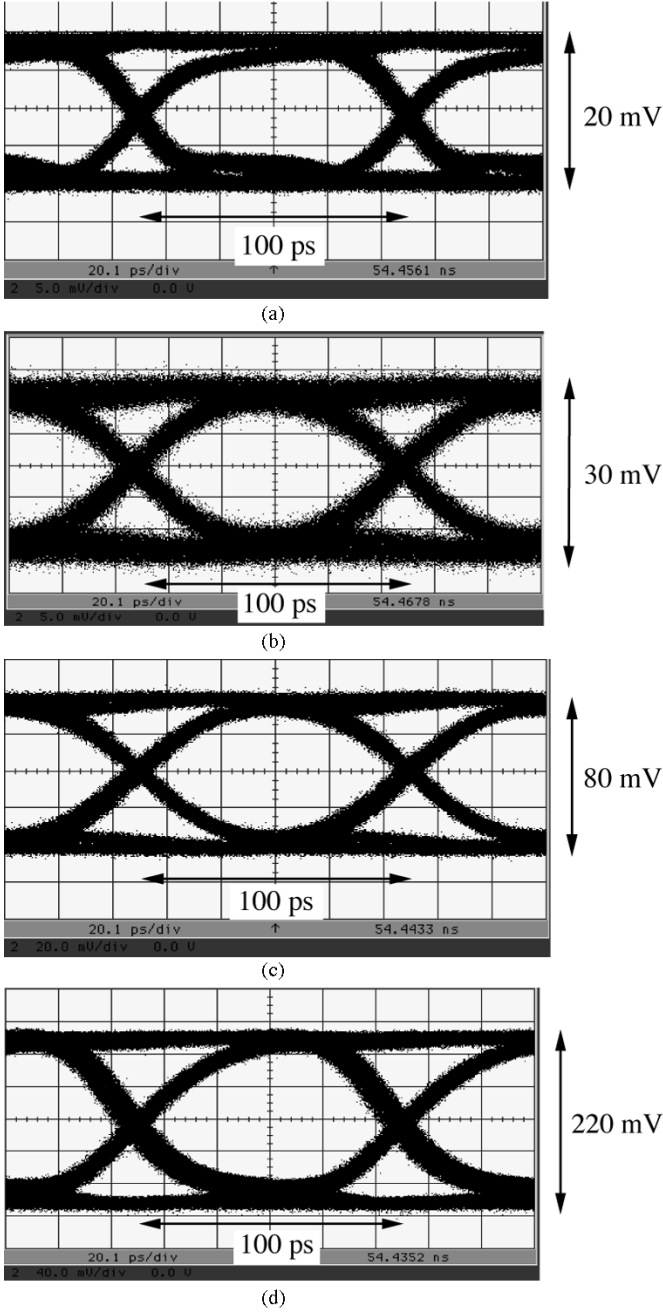


Fig. 12. Measured eye diagrams at 10 Gb/s: (a) through measurement at 20 mVpp and single-ended amplifier output for differential input signals of amplitude (b) 7 mVpp, (c) 20 mVpp, and (d) 400 mVpp.

achieved in this technology by sacrificing some core amplifier gain, and by reducing the gain of the output buffer.

VI. CONCLUSION

When used for optical transceiver applications, the CHEF amplifier must have high gain and bandwidth, low noise, and acceptable large-signal behavior. Design techniques for achieving all of these goals simultaneously were given in this paper. A pair of complex poles was found to dominate the amplifier frequency response. The relative values of resistors which result in optimum pole quality factor were described. Furthermore, the dominant noise sources in the amplifier were identified. A

19.7-dB gain, 13.7-GHz bandwidth implementation of the circuit verified the small- and large-signal behavior.

APPENDIX I AMPLIFIER DC TRANSFER CHARACTERISTIC

The notation labeled in Fig. 1 is used throughout this appendix. The parasitic emitter resistances of the HBTs will be ignored for simplicity. Using $I_{C2} - I_{C1} \cong I_{C2} - (I_{EE1} - I_{C2}) \cong 2I_{C2} - I_{EE1}$ and $I_{C4} - I_{C3} \cong 2I_{C4} - I_{EE2}$,

$$V_1 - V_2 \cong R_1(2I_{C4} - I_{EE2}) + V_{BE6} - V_{BE5} + R_f(2I_{C2} - I_{EE1}). \quad (13)$$

Next, it is noted that for transistor k

$$V_{BEk} \cong V_T \cdot \ln \left(\frac{I_{Ck}}{I_{ES}} \right) \quad (14)$$

where I_{ES} is the scaling current proportional to the base-emitter junction area for a given transistor. Using this equation for Q_1 and Q_2 and solving for I_{C1} and I_{C2} and comparing gives

$$I_{C2} \cong I_{C1} \cdot e^{-V_{in}/V_T} \cong \frac{I_{EE1}}{1 + e^{V_{in}/V_T}} \quad (15)$$

$$I_{C4} \cong \frac{I_{EE2}}{1 + e^{(V_1 - V_2)/V_T}}. \quad (16)$$

For purposes of simplification, it is noted that $I_{C5} \cong I_{C1} + I_{C3}/\beta_{DC}$ and $I_{C6} \cong I_{C2} + I_{C4}/\beta_{DC}$. Equation (1) is derived using (13)–(16) and using the tanh function expressed in exponential form.

Next, it is recognized that

$$V_{o1} - V_{o2} \cong (I_{C4} - I_{C3})(R_1 + R_2) \cong (2I_{C4} - I_{EE2})(R_1 + R_2). \quad (17)$$

Equation (2) is derived by substituting (16) into (17) and again using tanh expressed in exponential form. Equation (2) overestimates the slope of the transfer characteristic somewhat for small applied voltages because the parasitic HBT emitter resistances have been ignored here for simplicity. When these parasitics are included, one of I_{C1} or I_{C2} and one of I_{C3} or I_{C4} must be found iteratively.

APPENDIX II ANALYSIS OF THE EMITTER-FOLLOWER LOAD

The CHEF amplifier is usually followed by an emitter-follower output buffer. The amplifier will be loaded by the input impedance of the emitter-follower, Z_{inEF} , which in turn depends on the input impedance of the stage connected to the output of the emitter-follower. Fig. 13(a) shows one example, where the output of the emitter-follower is connected to a differential pair. The differential pair could represent the input to another CHEF amplifier stage, or a buffer to the output of the integrated circuit. Fig. 13(b) shows the high-frequency small-signal circuit of one emitter-follower and a differential-mode half circuit of the differential-pair input. Using this circuit, Z_{inEF} is given by

$$Z_{inEF} \cong \frac{Z_1}{sC_{\mu EF}Z_1 + 1} + r_{bEF} \quad (18)$$

current sources are open-circuited. Assuming $\beta \gg 1$, the output PSDs at nodes v_{o1} and v_{o2} due to $\overline{i_{c1}^2}$ are given by

$$\frac{\overline{v_{o1}^2(t)}}{\Delta f} = \frac{\overline{v_{o2}^2(t)}}{\Delta f} \cong \frac{\overline{i_{c1}^2} r_{d1}^2 (R_1 + R_2)^2 (R'_f + r_{d5})^2}{\Delta f 4r_{d1}^2 (R_1 + r'_{d3})^2}. \quad (22)$$

The mean square differential noise voltage between terminals v_{o1} and v_{o2} due to a given noise source is found for low frequencies to be

$$\begin{aligned} v_o^2 &= \overline{|v_{o1}(t) - v_{o2}(t)|^2} \\ &= \overline{v_{o1}^2(t) + v_{o2}^2(t) - 2v_{o1}(t)v_{o2}(t)} \\ &= \overline{v_{o1}^2(t) + v_{o2}^2(t)} - 2C_{12} \left| \overline{v_{o1}^2(t) \cdot v_{o2}^2(t)} \right|^{1/2} \end{aligned} \quad (23)$$

where $\overline{v_{o1}^2(t)}$ and $\overline{v_{o2}^2(t)}$ are the mean square noise voltages at nodes v_{o1} and v_{o2} respectively, and C_{12} is a measure of the correlation between $v_{o1}(t)$ and $v_{o2}(t)$ and always lies in the range $-1 \leq C_{12} \leq 1$. Substituting (22) into (23) with $C = -1$, since the noise voltages are anti-phase and fully correlated, results in $\overline{v_o^2(t)} = 4\overline{v_{o1}^2(t)}$. The noise current source $\overline{i_{c2}^2}$ contributes an equal amount of noise. The contributions of the remaining noise sources may be found in the same way.

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