A DC-6 GHZ, 50 DB DYNAMIC RANGE, SIGE HBT TRUE LOGARITHMIC AMPLIFIER

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ABSTRACT

In this work, a DC-6 GHz true logarithmic amplifier is presented. The amplifier uses a branch parallel summation architecture with four gain paths, and provides a piecewise approximate logarithmic response. The amplifier has 39 dB gain, 12.5 dB noise figure, 6.5 mV/dB logarithmic slope, and 50 dB logarithmic dynamic range. The amplifier uses Cherry-Hooper gain stages with emitter follower feedback. It also includes an on-chip automatic DC offset error reduction scheme. The circuit was fabricated in a 47 GHz SiGe HBT process. It draws 130 mA from a -3.3 V supply for a power consumption of 430 mW.

1. INTRODUCTION

Logarithmic amplifiers are widely used in radar receivers and in radio receivers as received strength signal indicators (RSSI). They are also used in instrumentation, and wherever a logarithmic function is required. Recently, it was shown how a logarithmic function may be used in a fiber optic transmitter as part of a broadband single-sideband fiber optic communication system [1, 2]. In this application, a high bandwidth 'true' or non-demodulating logarithmic amplifier is required. In addition, high dynamic range, small logarithmic error, and low noise are desirable features of the logarithmic amplifier in this or any other application.

In a previous work, the authors have described an amplifier architecture which provides a piecewise approximate logarithmic response while achieving high bandwidth [2]. Fig. 1 shows a block diagram of the logarithmic amplifier. This amplifier uses a parallel summation architecture, whereas previously published high frequency logarithmic amplifiers use the twin-gain stage architecture [3, 4]. Following the input buffer, there are four paths through which the signal can propagate to the output, labeled as G_{p1-4}. Path G_{p1} has nearly unity gain, and each successive path has a larger gain, with path G_{p4} having the highest gain. As the input signal amplitude is increased, the transconductance elements at the output of paths G_{p4} down to G_{p1} will sequentially limit. The factor increase in the input voltage between the point where one path limits and the next path limits is defined as A. In reference [2], a design procedure for choosing the path gains was given based on the choice of A, leading to an overall logarithmic dynamic range of A^4 for the amplifier. Furthermore, at the point where each transconductance element limits, the amplifier output voltage is proportional to the logarithm of its input voltage.

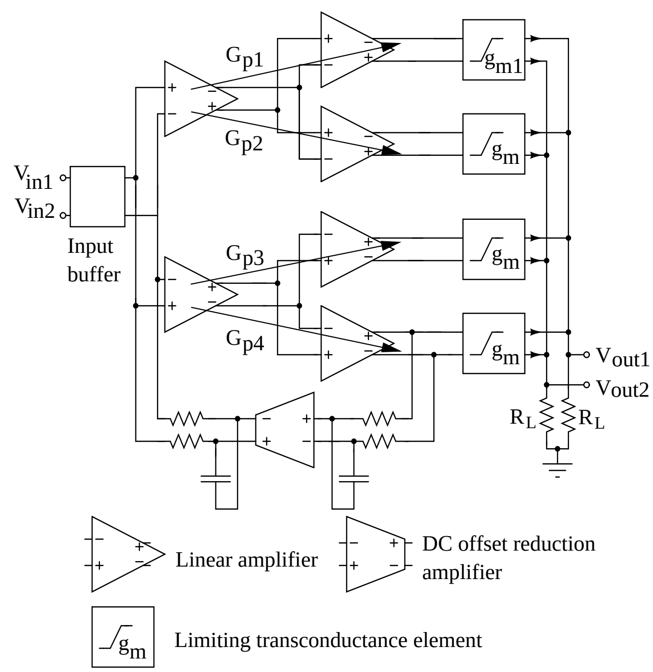

Fig. 1. Logarithmic amplifier block diagram.

The amplifier in [2] was a DC-4 GHz true logarithmic amplifier that operates at lower power than previously published high frequency true logarithmic amplifiers [3, 4]. This work presents a logarithmic amplifier which has 50% higher

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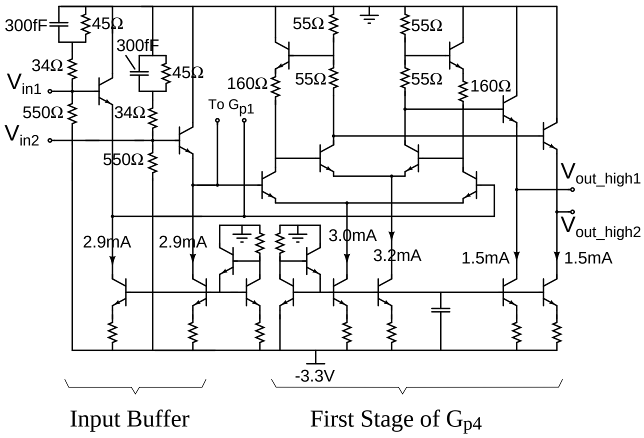


Fig. 2. Schematic diagram of the input impedance match circuit and first high gain stage.

bandwidth, 5.5× higher logarithmic slope, 10 dB higher logarithmic dynamic range, significantly lower noise figure, half of the chip area, and consumes 43% less power than the amplifier in [2]. Section 2 describes how a logarithmic transfer function is achieved using the circuit in Fig. 1. Section 3 describes a circuit implementation of the amplifier in a 47 GHz SiGe HBT technology along with measurements.

2. AMPLIFIER DESIGN

For the present design, the voltage gains G_{p1-4} were chosen as $G_{p1} = g_m/g_{m1}$, $G_{p2} = A-1$, $G_{p3} = A(A-1)$, and $G_{p3} = A^2(A-1)$, and $A = 5$. Each gain path is terminated in a limiting transconductance element with gain g_m and a maximum output current of $+/-\ I_L$, except the element at the output of path G_{p1} which has a gain of g_{m1} and a maximum output current of approximately $+/-\ AI_L/(A-1)$. For the present design $I_L = 6.7\ mA$. The sum of the output currents of the transconductance elements flows through resistors R_L in Fig. 1. The transfer characteristic describing the logarithmic response is given by [2]

$$V_{out1} - V_{out2} = 2R_L I_L \times \left[4 + \frac{A}{A-1} + log_A \left[\frac{g_m(V_{in1} - V_{in2})(A-1)}{A^2 I_L}\right]\right]. \quad (1)$$

The logarithmic amplifier was designed using DC coupled amplifier stages, as required by the optical transmitter application described in [2]. However, in order to achieve the full dynamic range, it is critical that some form of DC offset cancellation be used. In the circuit in Fig. 1, only the DC offset errors in the highest gain path G_{p4} are large enough to cause significant performance degradation. For this reason, an amplifier and a low pass filter network were used in negative feedback around path G_{p4} in order to reduce the DC offset error.

3. IMPLEMENTATION AND MEASUREMENTS

Fig. 2 shows the schematic diagram of the input buffer, as well as the first stage in the highest gain path G_{p4}. The input match uses resistors as well as a capacitor to lower the input impedance at high frequencies. This capacitor counteracts the effect of bond wire inductances and so the input remains impedance matched to $50\ \Omega$ within 10 dB up to approximately 9 GHz. Large emitter lengths were used in the emitter follower input buffers in order to achieve low base resistance and low noise. As well, the bias currents of these buffers were optimized for low noise. Following the input buffer in Fig. 2 is the first stage of the highest gain path G_{p4}. The noise figure of the logarithmic amplifier is completely dominated by the input buffer and this stage. This stage is a Cherry-Hooper amplifier with emitter follower feedback [5, 6]. The emitter lengths of the two input transistors to this stage were also chosen relatively large in order to achieve low noise. All of the amplifier gain stages use this circuit topology. Both of the gain stages in path G_{p4} are the same and were designed with a voltage gain of approximately 10. Furthermore, it should be noted that by using the Cherry-Hooper stage in Fig. 2 for all gain stages, the delay through each gain path was designed to be approximately the same, and no capacitive compensation was needed. Emitter degeneration was used in the input emitter coupled pair of each Cherry-Hooper stage in the lowest gain path to achieve low gain while maintaining high bandwidth. Both stages in the lowest gain path G_{p1} are exactly the same.

Fig. 3 shows the amplifier that was used in negative feedback around path G_{p4} in order to reduce the DC offsets. In order to achieve a high pass corner frequency of 500 kHz for the offset cancellation, a 1 nF off-chip capacitor was used.

The four limiting transconductance elements in Fig. 1 were all integrated into a single amplifier, shown in Fig. 4. When an input signal from one of the gain paths is applied to one of the degenerated emitter coupled pairs, it steers the bias current of that pair to the side with the highest applied voltage. When the applied voltage becomes large enough, the amount of current steered limits at $I_L = 6.7\ mA$, or $I_{L1} = 9.0\ mA$ for the pair connected to the output of path G_{p1}. The load resistor was chosen as 73 Ω so that when it is combined with the parasitic capacitance of the transistors and the inductance of an output bond wire, the impedance remains matched to $50\ \Omega$ within 10 dB to approximately 8 GHz. A negative power supply of -3.3 V was used so that the amplifier inputs and outputs may be directly coupled to a $50\,\Omega$ load. Emitter degeneration was used to reduce the gain of the summing circuit, thereby reducing DC offset errors at the output.

The circuit was implemented in a 47 GHz f_t SiGe pro-

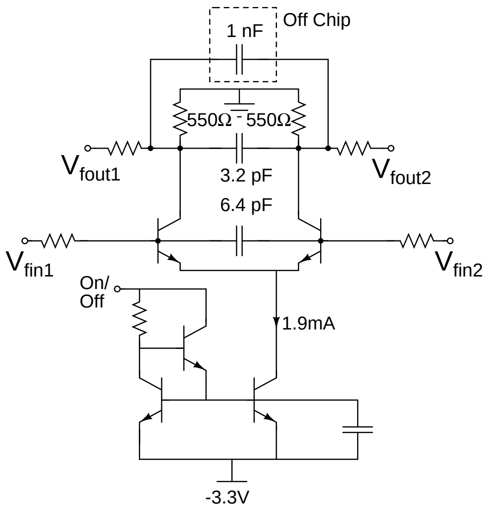


Fig. 3. Schematic diagram of the DC offset error reduction circuit.

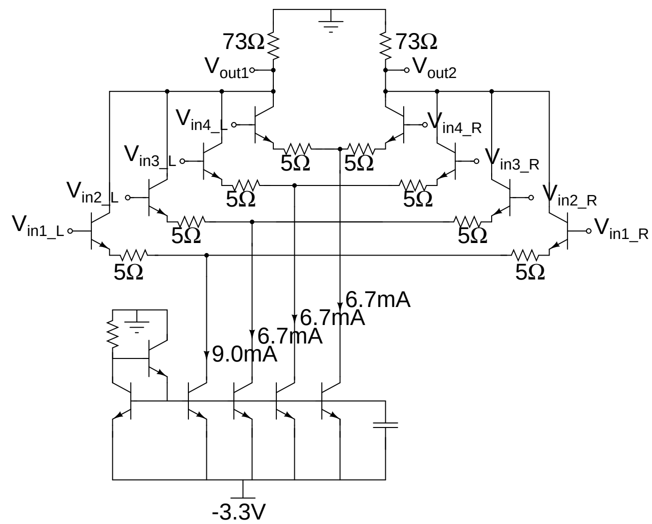


Fig. 4. Schematic diagram of the output summation circuit.

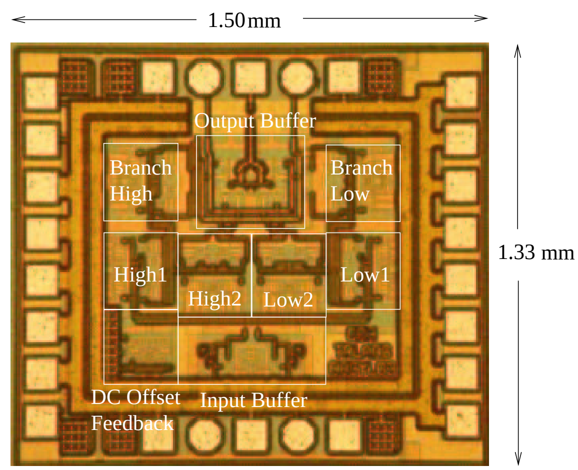


Fig. 5. Photograph of the integrated circuit.

cess. A photograph of the integrated circuit is shown in Fig. 5. The circuit draws 130 mA from the -3.3 V supply. The measured gain of the amplifier is 39 dB, compared to a simulated gain of 40 dB. The measured small signal bandwidth of the amplifier is 6 GHz, compared to 8 GHz simulated. It is expected that the inductance of the interconnect, which was not simulated, accounts for the lower measured bandwidth. The measured noise figure is 12.6 dB, which is the same as the simulated noise figure.

Fig. 6 shows the measured amplitude response of the amplifier for frequencies up to 6 GHz. The high logarithmic slope of 6.5 mV/dB was achieved by using relatively large currents in the output summing stage in Fig. 4. The logarithmic response error was calculated using the definition given in [2]. The log error at individual frequencies from 100 MHz to 6 GHz was less than 2.5 dB from an input power level of -52 dBm to -2 dBm. The error for frequencies from 100 MHz to 4 GHz when fit to a single line was less than 4.5 dB over the same input power range.

Fig. 7 shows the output waveforms for one of the two log amplifier outputs for frequencies of 100 MHz and 4 GHz. The rise and fall times of the amplifier are 50 ps. The logarithmic amplitude compression in the waveforms in Fig. 7 is evident. The observed noise at lower amplitude levels is partly due to amplifier noise and partly due to timing noise inherent in the sampling oscilloscope measurement.

Table 1 compares this amplifier with two other high frequency true logarithmic amplifiers. The amplifier in this work has higher bandwidth, logarithmic dynamic range, and logarithmic slope, while consuming less power.

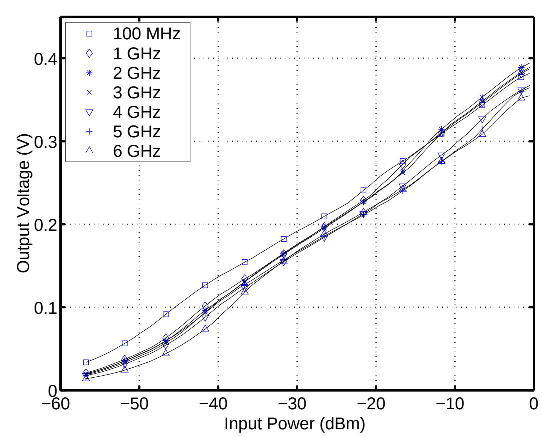
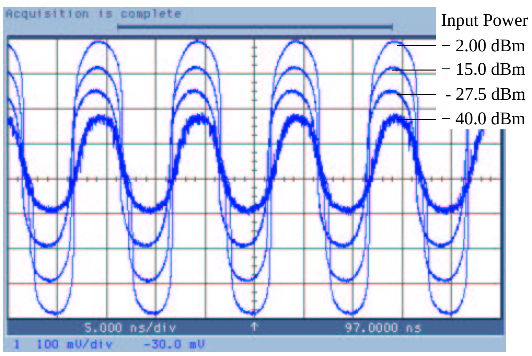


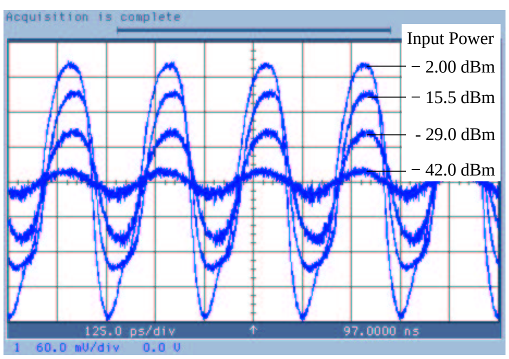
Fig. 6. Single ended logarithmic response from 100 MHz to 6 GHz.

Table 1. Comparison of Microwave True Logarithmic Amplifiers

Circuit	Topology	Technology	Power Supply	Gain	Band-width	Rise/ Fall Time	Dyna-mic Range	Log Slope
Oki *et al.*[3]	Twin-Gain Stage	GaAs HBT	-8 V 1.06 W	48dB	DC- 3 GHz	400 ps/ 400 ps	40 dB	3.3 mV/dB
Holdenried *et al.*[2]	Branch Parallel Summation	Si Bipolar f_t =35 GHz	-5 V 0.75 W	30 dB	DC- 4 GHz	100 ps/ 100 ps	40 dB	1.2 mV/dB
This Work	Branch Parallel Summation	SiGe HBT f_t =47 GHz	-3.3 V 0.43 W	39 dB	DC- 6 GHz	50 ps/ 50 ps	50 dB	6.5 mV/dB



(a) Logarithmic response at 100 MHz



(a) Logarithmic response at 4 GHz

Fig. 7. Real time logarithmic amplifier single ended output waveforms.

4. CONCLUSIONS

An enhanced parallel summation logarithmic amplifier was presented. It uses Cherry-Hooper amplifier stages with emitter follower feedback in order to achieve high bandwidth and to achieve matched signal delay among the four gain paths. The amplifier was optimized for low noise and for high logarithmic slope. This work shows that the branch parallel summation architecture provides high bandwidth and logarithmic slope while consuming relatively low power.

5. REFERENCES

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