

A DC-6 GHz, 50 dB Dynamic Range, SiGe HBT True Logarithmic Amplifier

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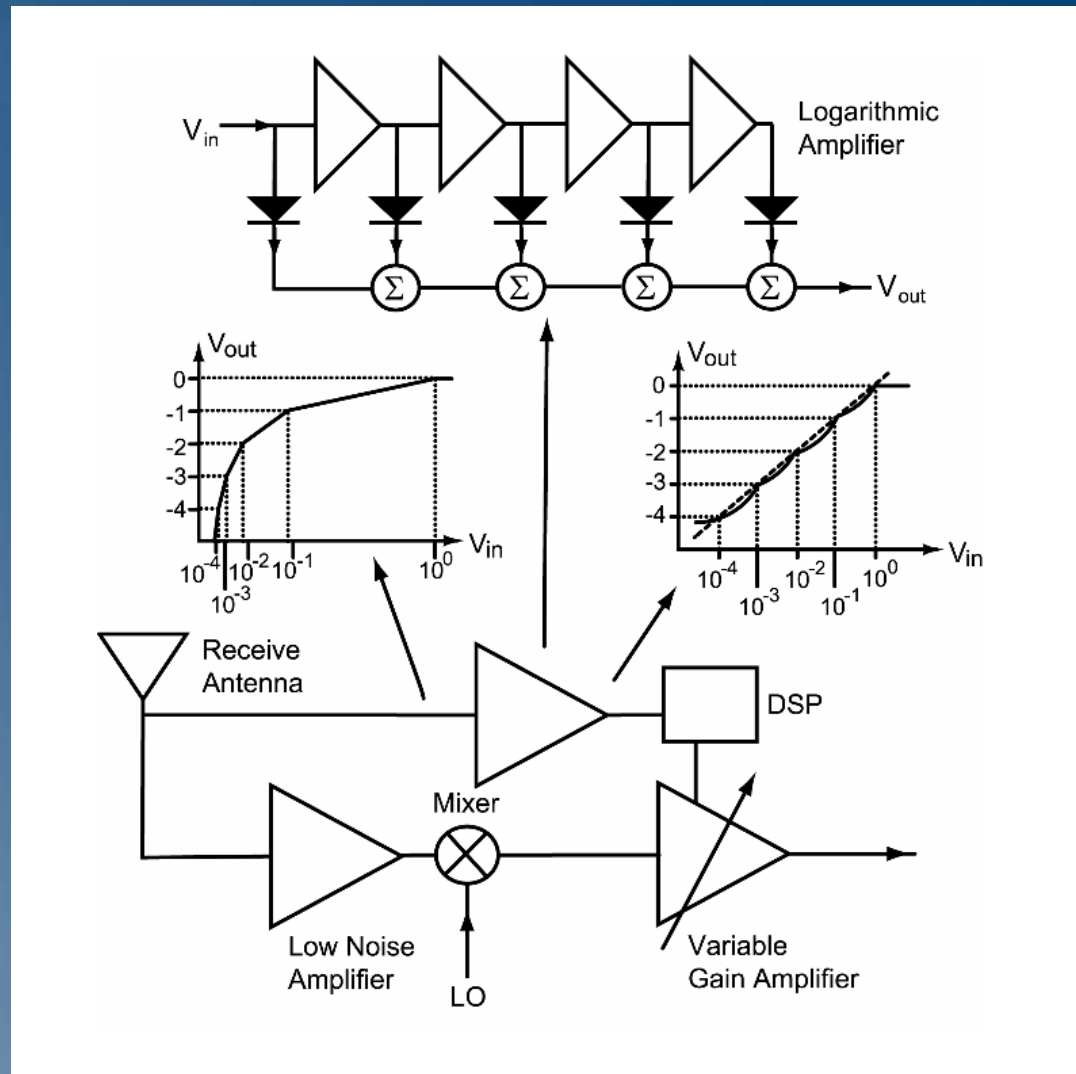


Outline

- Logarithmic amplifier applications
 - Received Strength Signal Indicator (RSSI)
 - Compatible Optical Single Sideband (COSSB)
- Logarithmic amplifier architectures
 - Series linear-limit
 - Parallel summation
- Design
- Measurements
- Conclusion

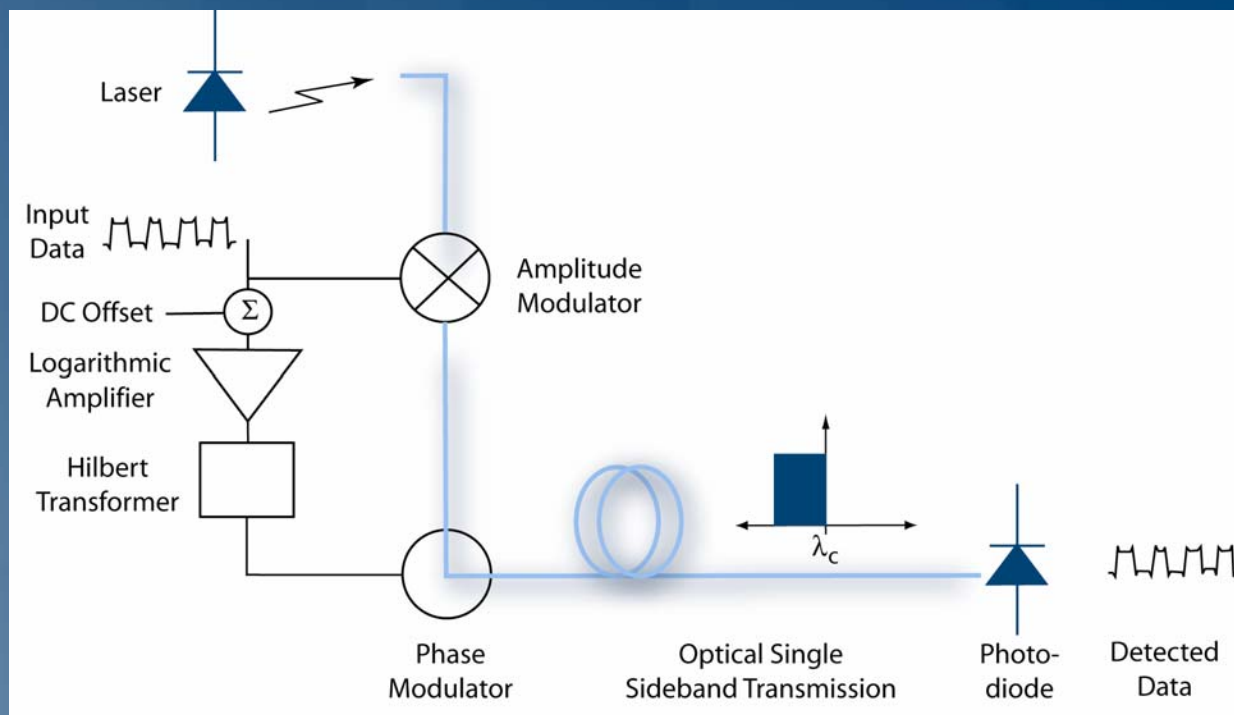
Traditional Application: RSSI

- Receive strength signal indicator (RSSI).
- Requires a demodulating logarithmic amplifier.
- Piecewise approximate response.
- Key requirements:
 - Very low power.
 - High dynamic range.



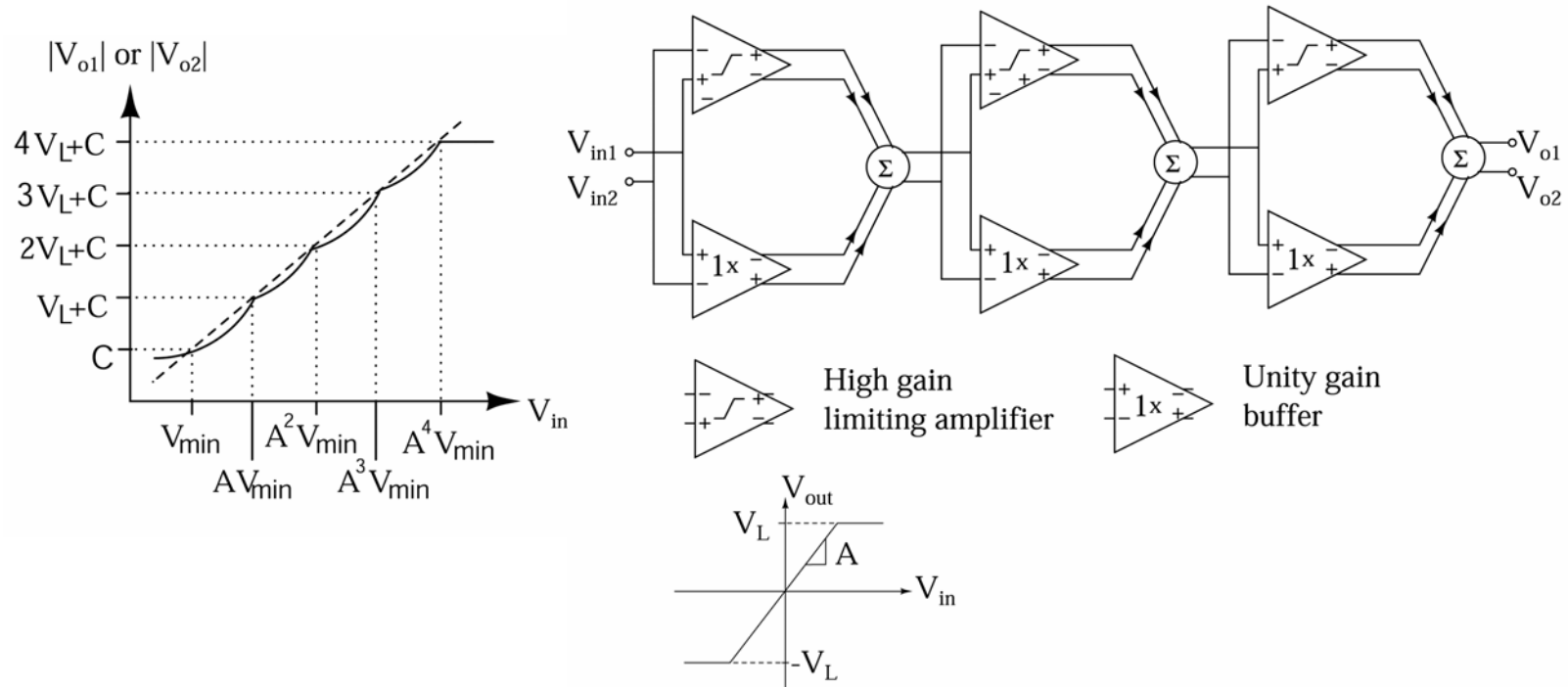
Unique Application: Compatible Optical Single Sideband (COSSB)

- Log amplifier used in optical transmitter.
- Used in generating SSB.
- Key requirements:
 - High bandwidth.
 - Low noise.
 - High logarithmic slope.



COSSB System
(Holdenried et al., Wireless 2001)

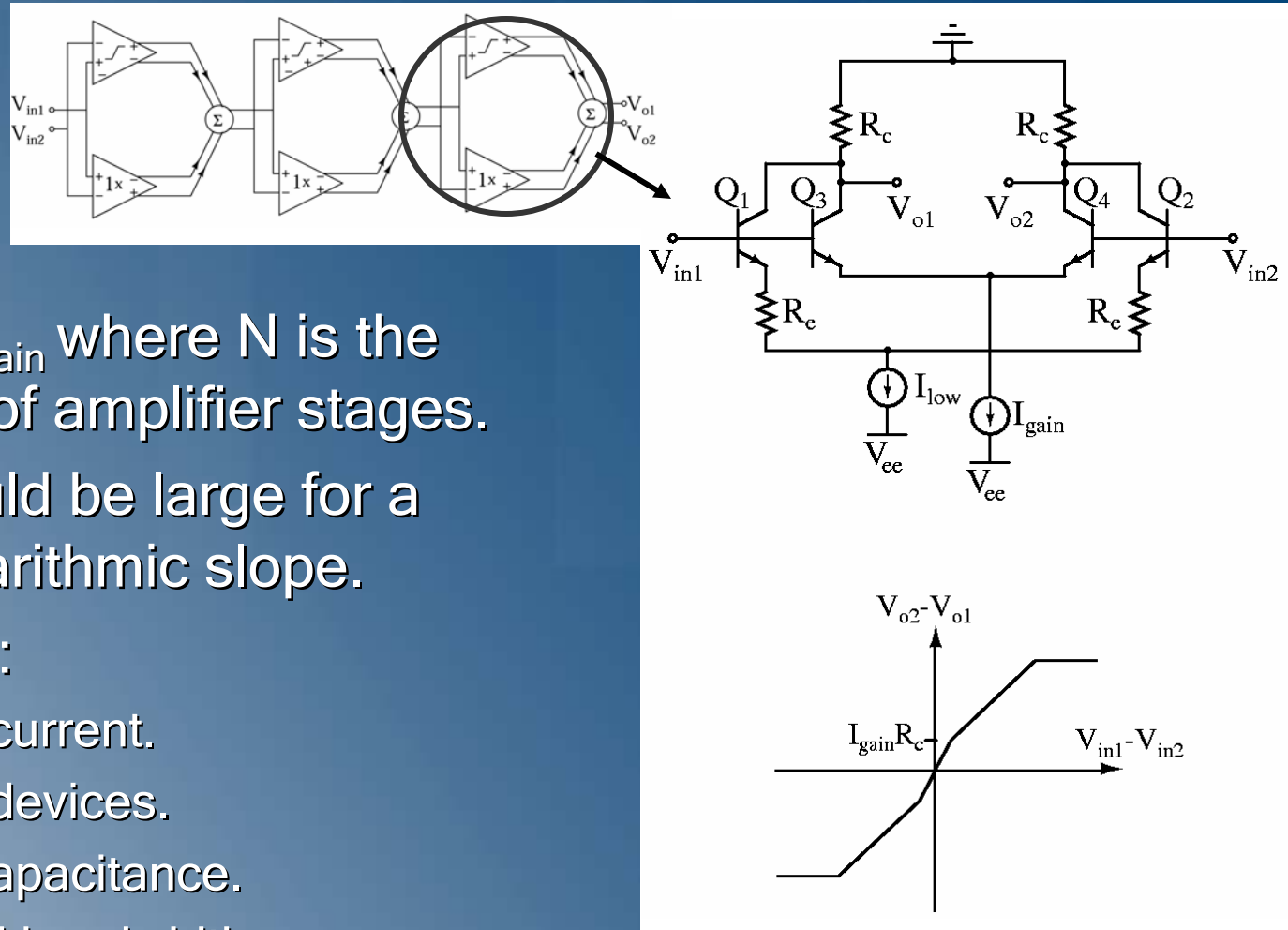
Twin-Gain Stage Architecture



(Barber and Brown, J. Solid State Circuits, 1980)

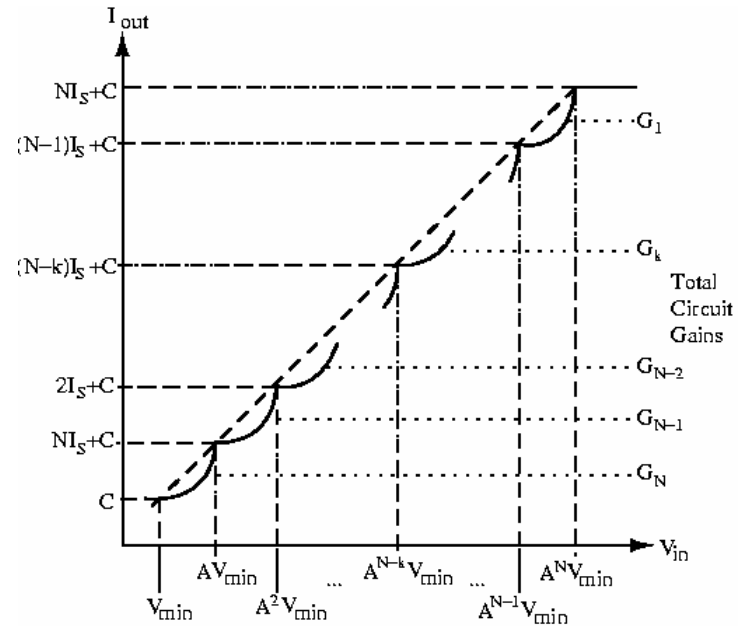
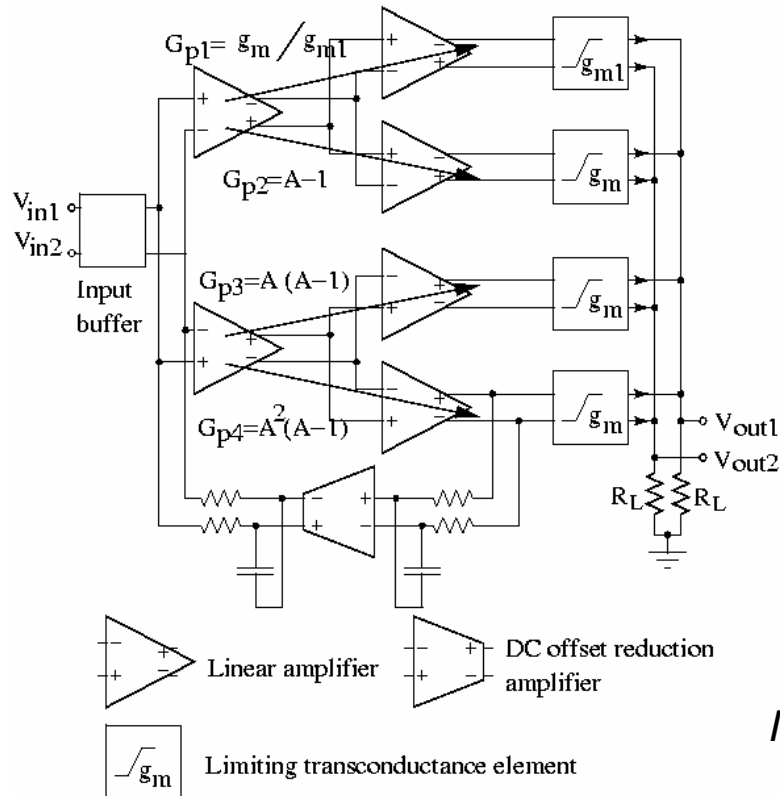
- Gain stages limit as input signal becomes large.
- Unity gain buffers continue to pass the signal.

Twin-Gain Stage Implementation



- $I_{low} > N I_{gain}$ where N is the number of amplifier stages.
- I_{gain} should be large for a high logarithmic slope.
- Leads to:
 - Large current.
 - Large devices.
 - High capacitance.
 - Limited bandwidth.

Logarithmic Amplifier Block Diagram



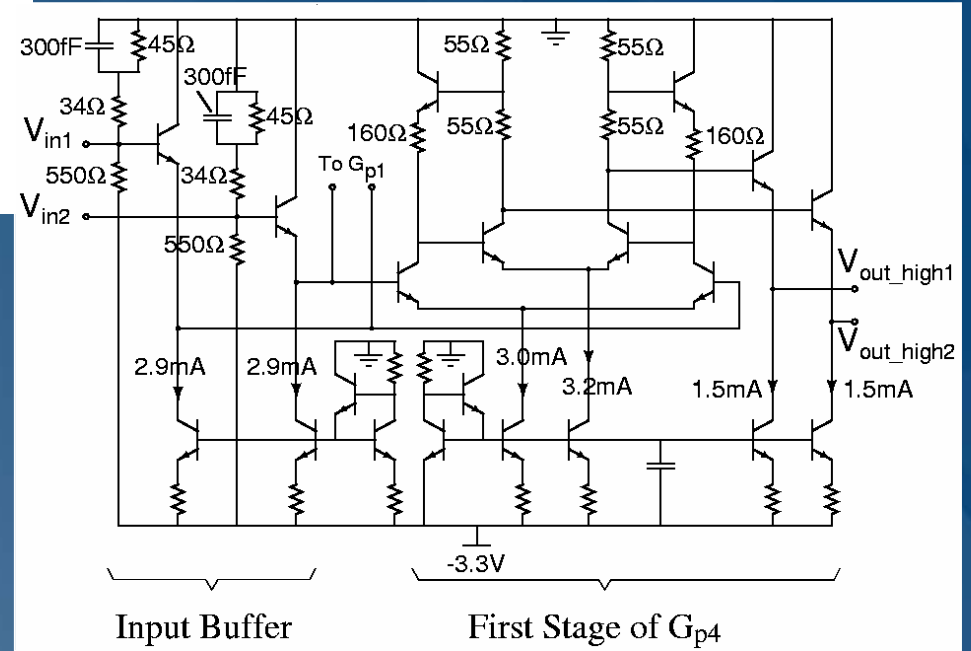
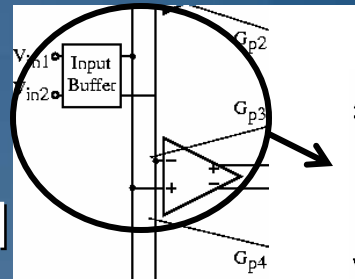
$$I_{out} = I_L \left[4 + \frac{A}{A-1} + \log_A \left[\frac{g_m (V_{in1} - V_{in2})(A-1)}{A^2 I_L} \right] \right]$$

(Holdenried et al., J. Solid State Circuits, 2002)

- Parallel architecture developed at TRILabs, patent pending.
- Response is a piecewise approximation to a logarithm.

Amplification Stage: Cherry-Hooper Amplifier with Emitter Follower Feedback

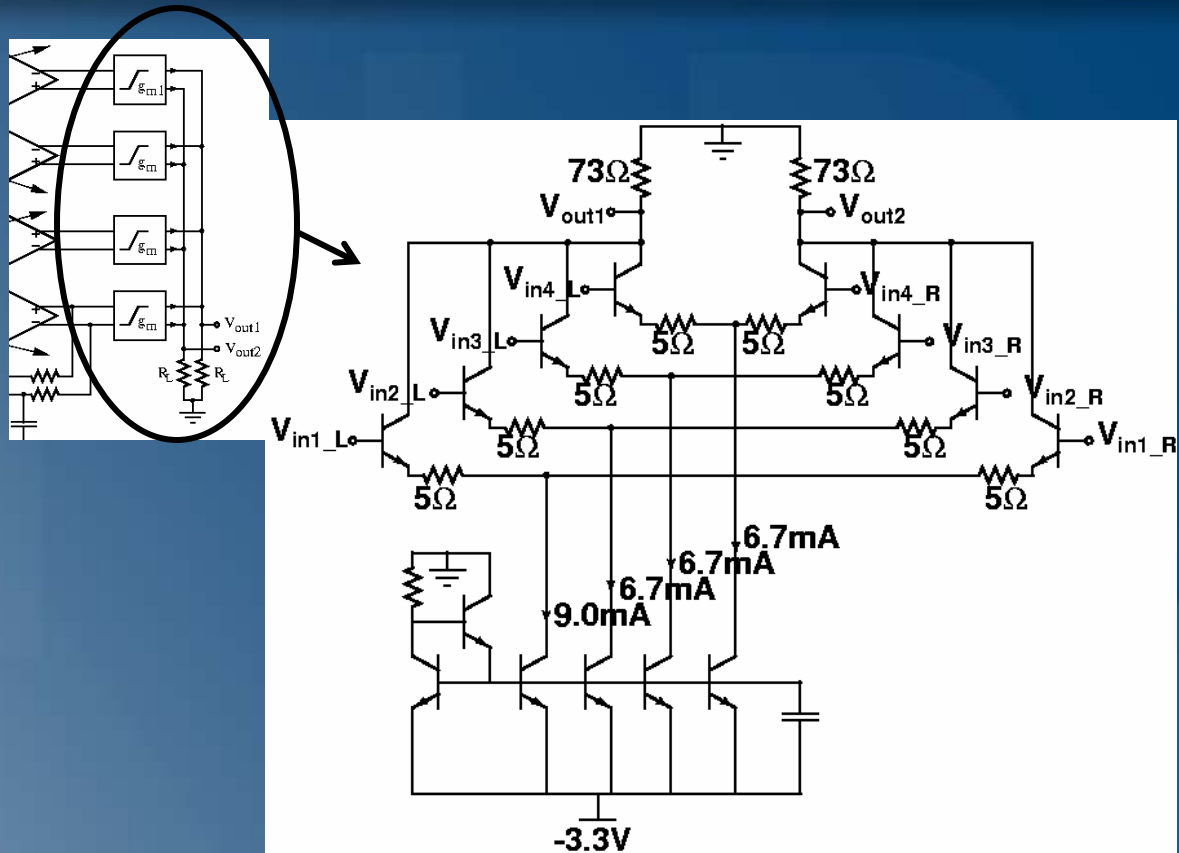
- Amplifier topology commonly used in 40 Gb/s receivers.
- Each stage has 20 dB gain, 10.4 GHz bandwidth.
- Designed for high bandwidth and low group delay distortion.



Input Buffer and One Amplifier Stage

Logarithmic Amplifier Summing Stage

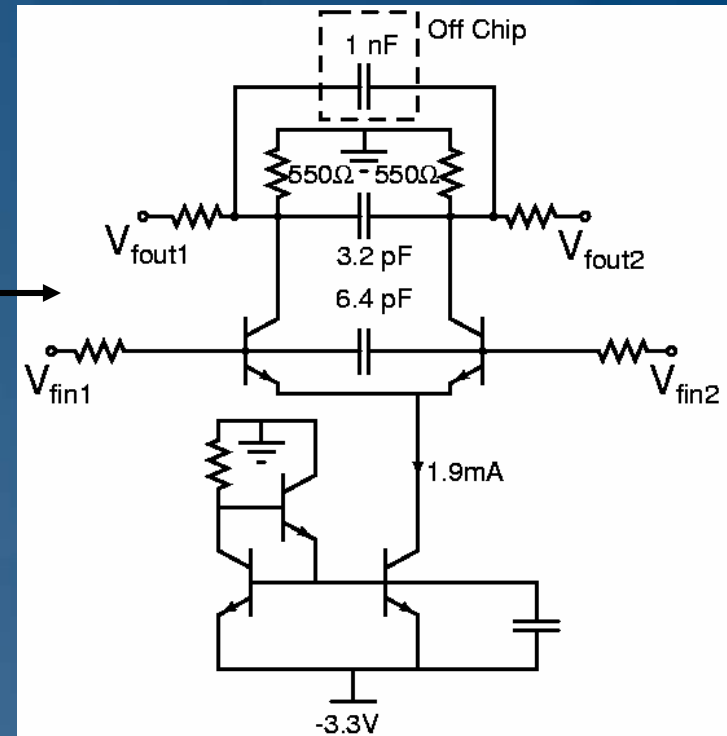
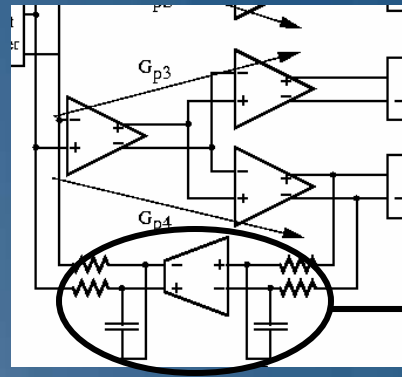
- Limiting function provided by differential pairs.
- Currents sum through output resistors.
- Large currents used to drive the load.



Limiting/Summing Stage

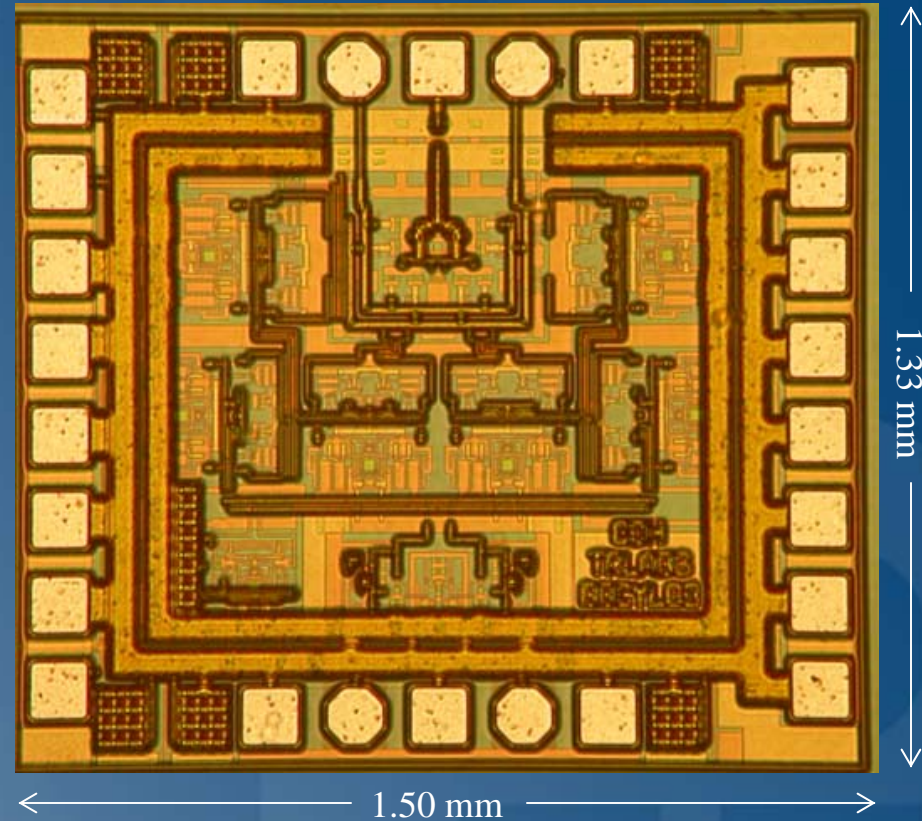
DC Offset Error Feedback Amplifier

- Differential pair amplifier.
- Uses off chip capacitor to achieve 3 dB cutoff below 1MHz.



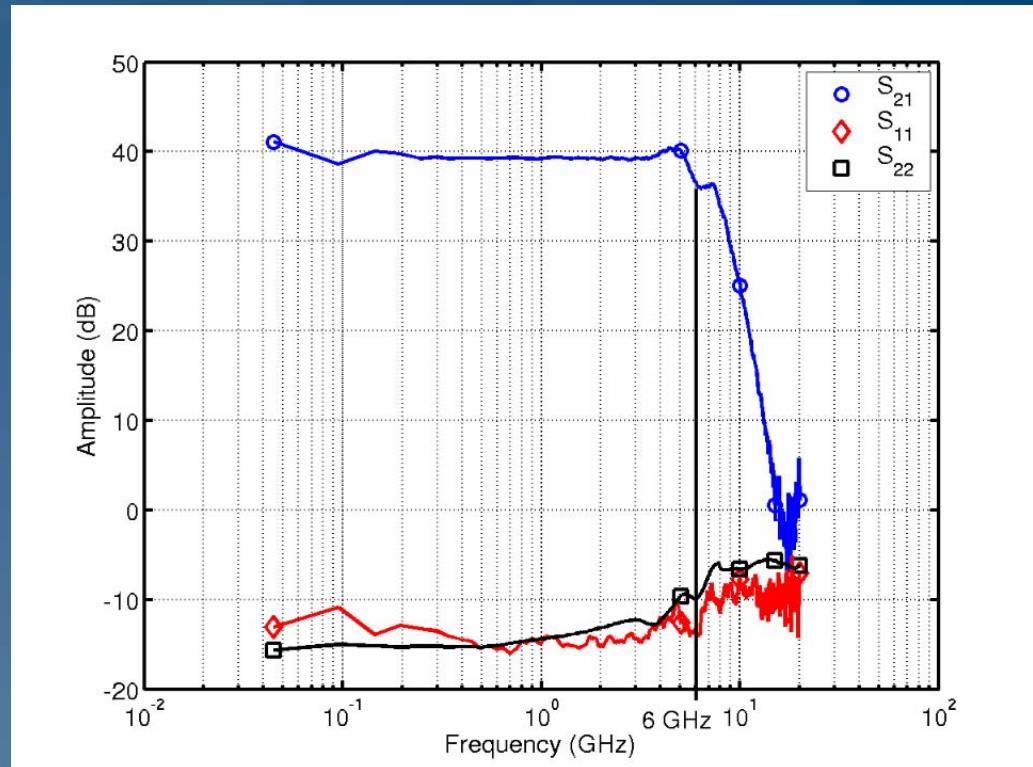
Logarithmic Amplifier Micro-Photograph

- Fabricated in IBM HP5 47 GHz SiGe HBT technology.
- Draws 130 mA from -3.3 V supply.
- Third generation design.



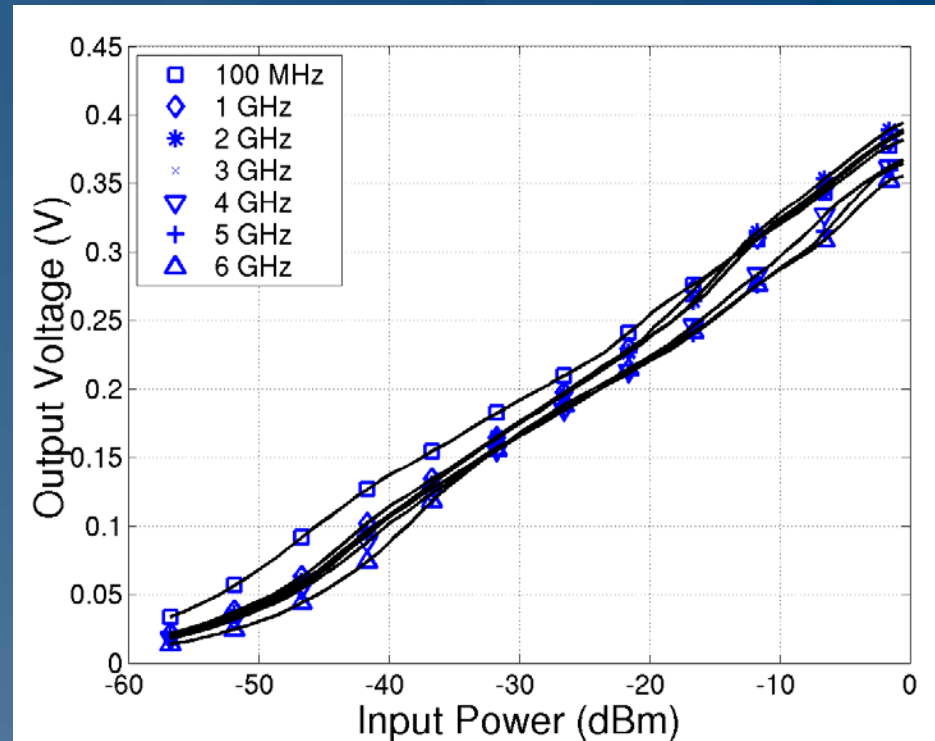
Small Signal Performance

- DC-6 GHz bandwidth.
- 39 dB single-ended small signal gain.
- S_{11} and S_{22} below -10dB up to 6 GHz.
- 12.5 dB measured noise figure.



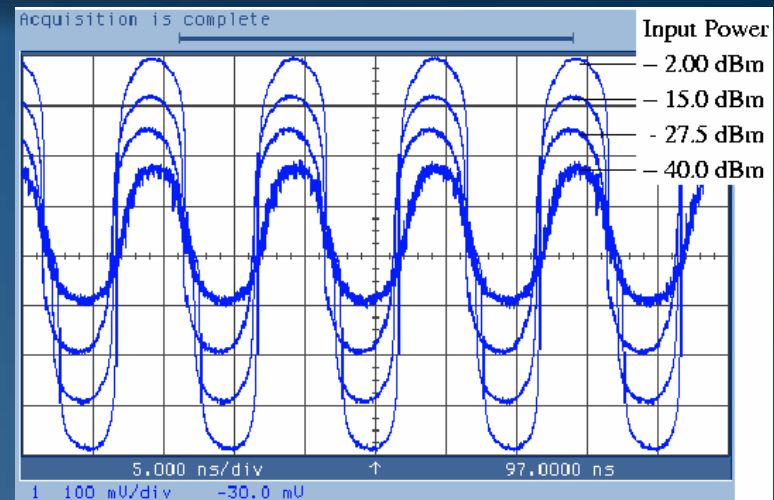
Logarithmic Amplifier 1-Tone Test

- 50 dB of logarithmic dynamic range.
- ± 2.5 dB log conformity error at individual frequencies.

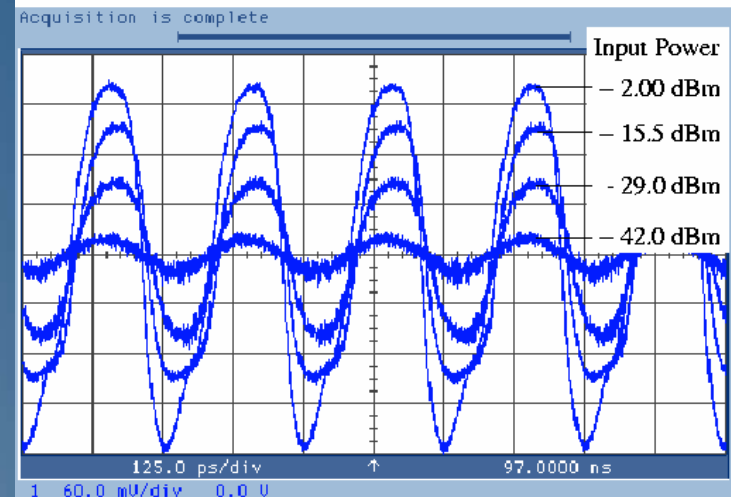


Logarithmic Amplifier Waveforms

- 50 ps rise/fall times.
- Greater than 800mVpp single-ended output swing.



Logarithmic response at 100 MHz

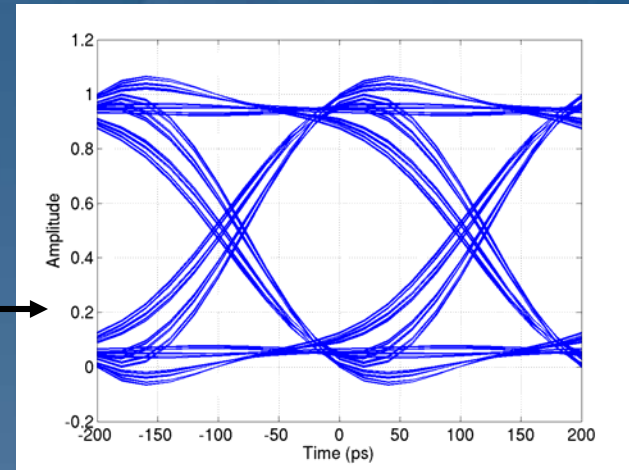
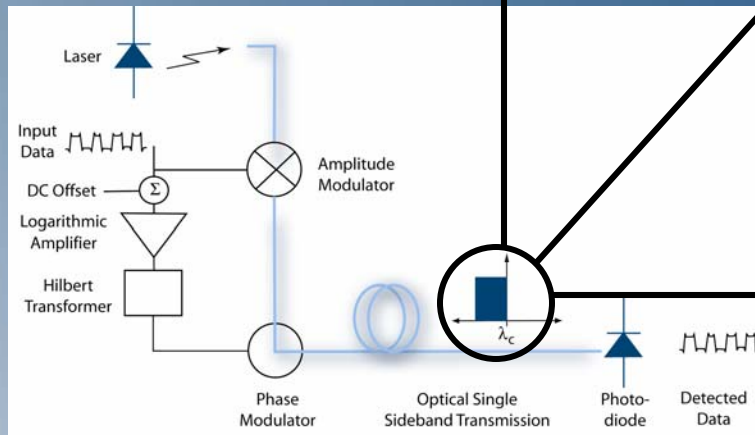
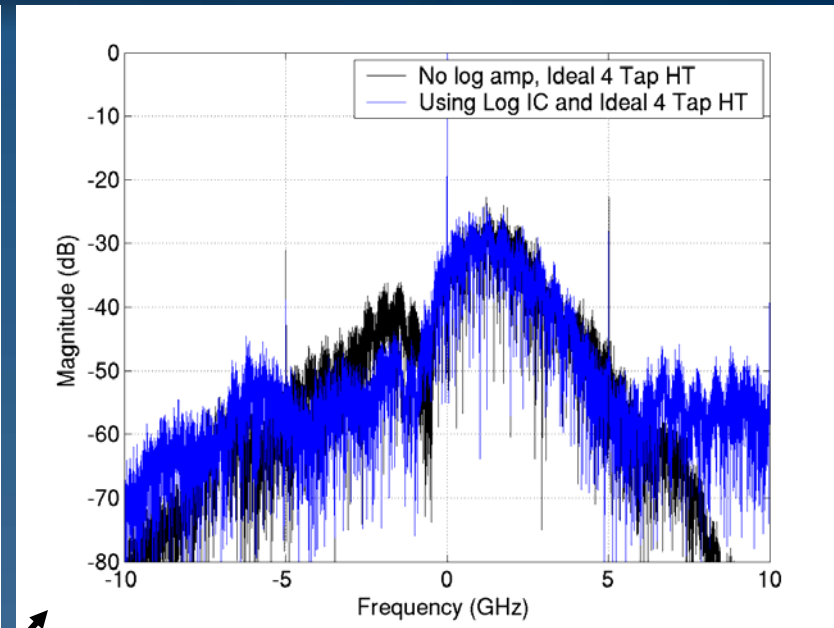
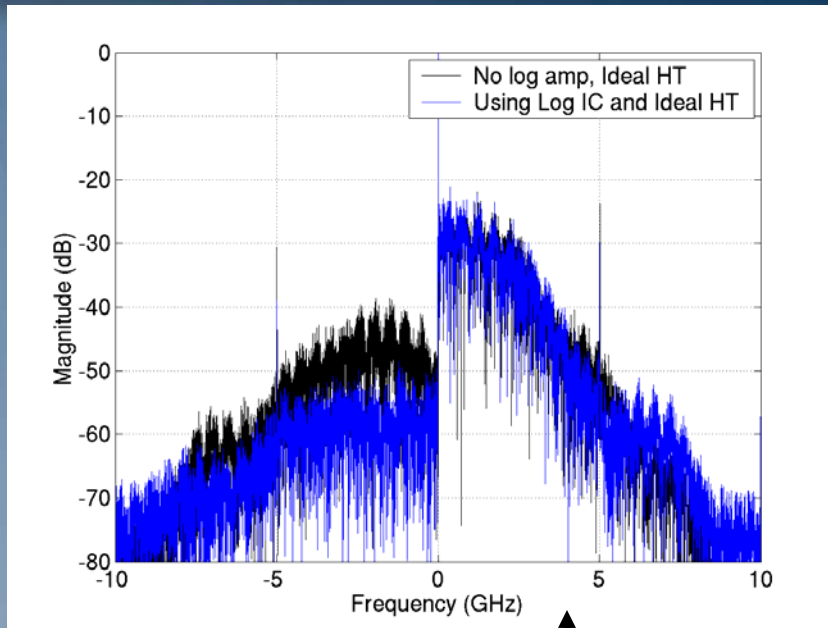


Logarithmic response at 4 GHz

Comparison of Logarithmic Amplifiers

Circuit	Topology	Technology	Power Supply	Gain	Band-width	Rise /Fall Time	Dynamic Range	Log Slope
Acciari <i>et al.</i>	Twin-Gain Stage	GaAs FET	-	36 dB	0.3-5 GHz	-	40 dB	10 mV/dB
Smith	Twin-Gain Stage	GaAs FET Hybrid Circuit	-8 V, +8 V 5.2 W	70 dB	0.5-4 GHz	-	70 dB	6.3 mV/dB
Oki <i>Et al</i>	Twin-Gain Stage	GaAs HBT	-8 V 1.06 W	46 dB	DC-3 GHz	400 ps/ 400 ps	40 dB	3.3 mV/dB
Holdenried <i>et al.</i>	Branch Parallel Summation	Si Bipolar $f_t = 35\text{GHz}$	-5 V 0.75 W	30 dB	DC-4 GHz	100 ps/ 100 ps	40 dB	1.2 mV/dB
Holdenried <i>et al.</i>	Branch Parallel Summation	SiGe HBT $f_t = 47\text{GHz}$	-3.3 V 0.43 W	39 dB	DC-6 GHz	50 ps/ 50 ps	50 dB	6.5 mV/dB

Simulation of a 5 Gb/s COSSB Signal



Logarithmic Amplifier Performance Summary

Supply Voltage	-3.3 V
Current Draw	130 mA
Power Consumption	430 mW
Bandwidth	6 GHz
Single-Ended Gain	39 dB
Logarithmic Dynamic Range	50 dB
Logarithmic Slope	6.5 mV/dB
Logarithmic Error	± 2.5 dB
Rise/Fall Time	50 ps/ 50 ps
Noise Figure	12.5 dB

Conclusion and Acknowledgements

Conclusion

- Optical transceiver application requires high bandwidth logarithmic amplifier.
- Traditional series architecture has a logarithmic slope/bandwidth tradeoff.
- Parallel summation architecture alleviates this tradeoff.

Acknowledgements

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