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A DC–4-GHz True Logarithmic Amplifier: Theory and Implementation

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Abstract—A 40-dB dynamic range, dc–4-GHz parallel-summation logarithmic amplifier is presented in this paper. The amplifier realizes a piecewise approximation to an exact logarithmic response. A design procedure that yields breakpoints on the exact response is described, along with delay-matching networks for parallel-summation logarithmic amplifiers. The amplifier was constructed in a 35-GHz silicon bipolar process, has ± 5 dB logarithmic conformity over a dc–4-GHz bandwidth and has rise and fall times of 100 ps. The integrated circuit has dimensions of 2×2 mm² and consumes 750 mW from a –5-V supply.

Index Terms—Gain control, logarithmic amplifiers.

I. INTRODUCTION

LOGARITHMIC amplifiers are widely used in radar receivers to compress the high dynamic range of received signals. They were developed, in part, out of the need to replace automatic gain control (AGC) circuits with a higher dynamic range circuit. The scattering and multipath experienced by radar signals can result in variations in received input power of over 100 dB. Some logarithmic (log) amplifiers have a logarithmic dynamic range greater than this, and bandwidths that are comparable to AGC circuits. Furthermore, logarithmic amplifiers are used in monopulse direction finders [1] and other circuits for radar and tracking.

The applications of log amplifiers extend beyond their use in radar and radio. The all presented the use of a logarithmic amplifier in a fiber-optic receiver [2]. In that work, a logarithmic amplifier was used as a form of gain control in the receiver to counteract the effects of bias point drift in the transmitting laser and the receiver photodiode. Logarithmic amplifiers suit this application well because of their high bandwidth and fast response time. However, the use of log amplifiers in fiber-optic networks is not limited to the receiver. A new application of log amplifiers, shown in Fig. 1, involves the generation of optical single-sideband signals. The log amplifier is used in series with a Hilbert transformer to generate an electrical signal that, when

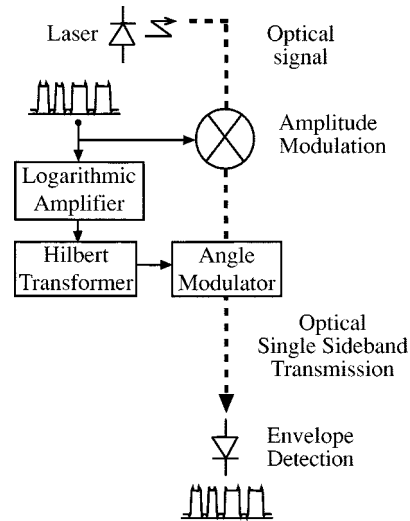


Fig. 1. Phase-modulation-based optical single-sideband system.

used to angle modulate the optical signal, generates an optical single-sideband signal which may be envelope detected. This technique is particularly well suited to high-data-rate baseband signals [3]–[5].

In this paper, logarithmic amplifiers are described that are suitable for use in fiber-optic applications and radar applications with narrow pulsewidths. Fiber-optic applications, in particular, require logarithmic amplifiers that meet a unique set of requirements. In the application shown in Fig. 1, the input signal is a baseband signal which is strictly positive, and so it has dc and low frequency components which must be logged. Hence, the logarithmic amplifier should be dc coupled throughout. As well, maximizing the bandwidth of the logarithmic amplifier is critical, because of the high data rates. Additionally, not only must the log amplifier operate over a large range of frequencies, but the random nature of the data dictates that all frequencies are in use simultaneously. Consequently, it is important that variations in the group delay throughout the passband remain small compared to the bit period of the data being transmitted. This paper presents logarithmic amplifiers that feature low group-delay distortion.

In Section II, the various types of logarithmic amplifiers are considered, with the goal of choosing a suitable topology for use in a fiber-optic network. A bandwidth limitation of the series linear-limit logarithmic amplifier topology is considered, and parallel-summation logarithmic amplifiers, which overcome this limitation, are described. In Section III,

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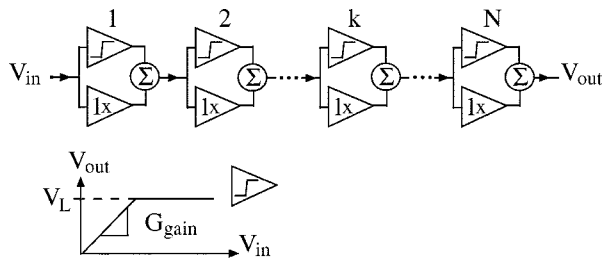


Fig. 2. Series linear-limit logarithmic amplifier.

a unified design procedure for parallel-summation logarithmic amplifiers is given. In Section IV, the design and operation of a novel dc-4-GHz logarithmic amplifier are described.

II. DISTINCTION AND COMPARISON OF LOGARITHMIC AMPLIFIER TYPES

There are two basic types of logarithmic amplifiers, the true and the demodulating types. True logarithmic amplifiers, also known as “baseband” or “video” logarithmic amplifiers, provide the logarithm of the signal without detecting or demodulating the signal. In contrast, demodulating logarithmic amplifiers provide the logarithm of the envelope of a signal.¹ This paper deals with the design of high-frequency true logarithmic amplifiers.

Logarithmic amplifiers may be further subdivided into single-stage and piecewise approximate types. Transconductance feedback log converters are based on an amplifier with a p-n junction or a MOSFET device in subthreshold in feedback around the amplifier [1]. These converters provide an excellent logarithmic response in low-frequency applications. A technique that has been more successful at high frequencies is the piecewise approximation of a logarithm, and this is the technique used in this work.

A. The Series Linear-Limit Logarithmic Amplifier

Fig. 2 shows the most widely used high-frequency true logarithmic amplifier topology. The amplifier consists of a cascade of dual gain cells, with each cell having a high-gain limiting amplifier in parallel with a unity-gain buffer. For small signals, this structure will simply amplify. However, as the signal becomes larger, a point will be reached at which the limiting amplifier in the last stage ceases to amplify and provides a constant voltage V_L . As the input signal becomes larger, the limiting amplifiers will successively reach their upper bound, starting with the second-last stage and progressing toward the input. Meanwhile, the buffer amplifiers in all stages will continue to pass the signal. This response, shown in Fig. 3, approximates a straight line when plotted on a semilogarithmic axis. A mathematical description of this amplifier’s operation is given in [7].

The series linear-limit topology is attractive because process variations, such as a low current gain for the transistors on a given wafer, will likely affect all stages more or less equally. If the gain of all of the stages is lower than expected, the only result

¹Exceptions are those circuits that may operate in the true *and* demodulating modes through the use of Gilbert-cell multipliers [6].

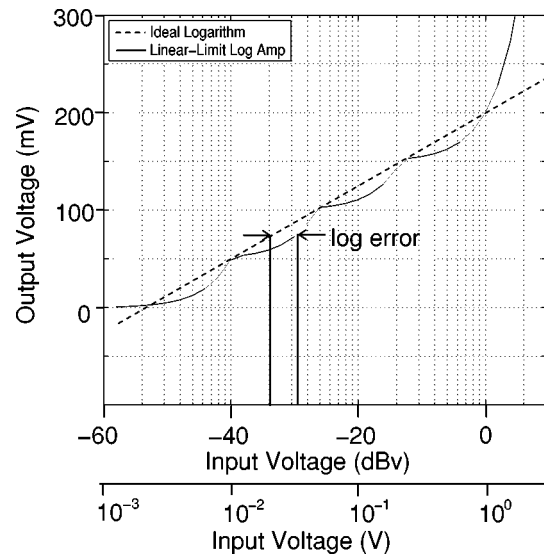


Fig. 3. Linear-limit logarithmic amplifier response.

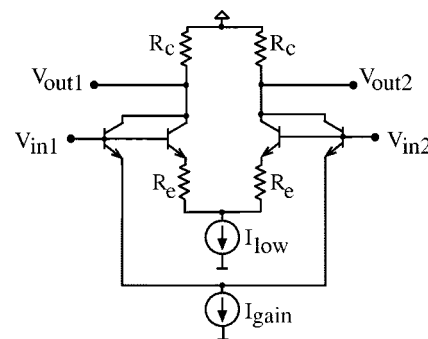


Fig. 4. High-gain limiter and unity-gain buffer in parallel.

is a scaling of the overall response, without affecting the logarithmic characteristic. The linear-limit topology is also simple, since more stages may be added in cascade if increased dynamic range is required, provided that the low-gain path in each stage does not saturate.

The requirement that the low-gain buffer amplifiers not saturate presents a challenge in designing the twin-gain stages. A common implementation consists of two differential pairs in parallel with shared collector nodes, as shown in Fig. 4 [7]–[9]. One differential pair uses emitter degeneration to provide low gain and the other differential pair is undegenerated to provide high gain.

Since the buffer amplifier in the N th stage must buffer the signal generated by stages 1 to $N - 1$, the requirement on I_{low} with respect to I_{gain} may be found to be [7]

$$\frac{I_{low}}{I_{gain}} > N. \quad (1)$$

However, I_{gain} needs to be somewhat large in order to achieve the desired gain. Therefore, (1) indicates that I_{low} will be large, necessitating large devices with high parasitic capacitance. These capacitances, in turn, will place bandwidth limitations on the series linear-limit logarithmic amplifier. One way to mitigate this difficulty is to lower the gain of the buffer amplifiers below unity so that they require a higher input voltage in order to limit, and so their current may be reduced. The gain may

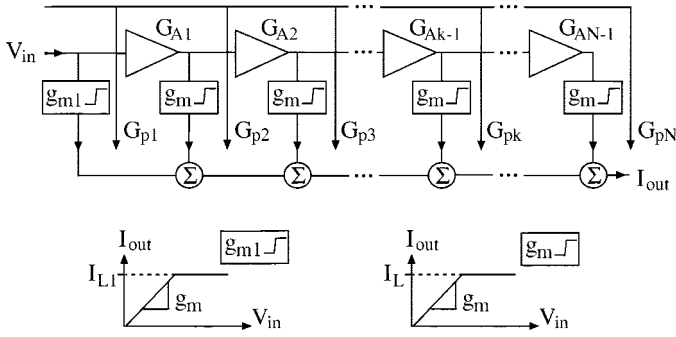


Fig. 5. Progressive-compression parallel-summation logarithmic amplifier.

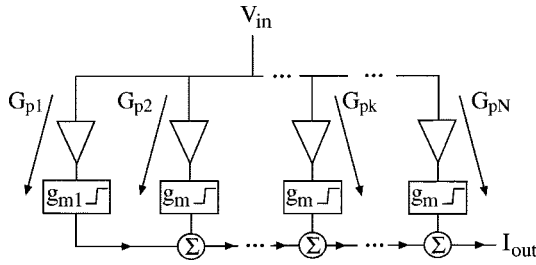


Fig. 6. Parallel-amplification parallel-summation logarithmic amplifier.

be lowered using increased emitter degeneration or a series resistor connected to the base of the buffering transistors [8].

Even if the size of the transistors in the buffer amplifier is reduced, the parasitic capacitance of the buffer amplifier will still load the gain amplifier in parallel with it. There is another class of log amplifiers where the high- and low-gain paths are separate. These are known as parallel-summation log amplifiers, which are described in Section II-B.

B. Parallel-Summation Logarithmic Amplifiers

The second class of log amplifiers is the parallel-summation type. Parallel-summation log amplifiers may be divided into the progressive-compression type and the parallel-amplification type. Each of these will be discussed in turn.

Fig. 5 shows a progressive-compression log amplifier [10]. Functionally, it is exactly the same as the series linear-limit amplifier, except that instead of sequentially summing and buffering the clipped outputs of each stage, the stage outputs are summed in parallel. In the progressive-compression amplifier, each component amplifier output voltage is converted to a current using a transconductance element. The transconductance elements provide current up to a maximum level, at which point their output current limits.

Another type of parallel-summation log amplifier is shown in Fig. 6, where it is seen that the component signals are generated in parallel. This topology exhibits high symmetry among the different paths. Hence, although the logarithmic dynamic range is lower, the phase and group-delay matching are inherently improved compared to the progressive-compression topology.

Comparing the two parallel-summation topologies, it is seen that the progressive-compression structure has the advantage of using multiple cascaded amplifiers to achieve high logarithmic dynamic range. As a result, the progressive-compression structure is widely used in log amplifier designs, for example, in [6] and [11]. The parallel-amplification scheme is efficient in low

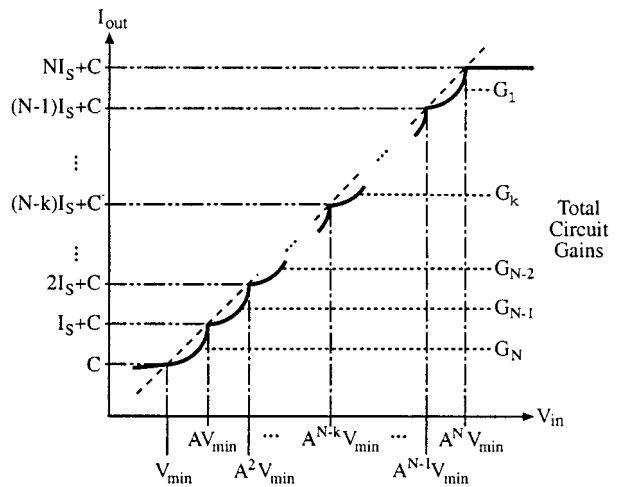


Fig. 7. Parallel-summation logarithmic amplifier transfer function.

dynamic-range applications, and has been used in works such as [12] and [13]. However, a mathematical design procedure has yet to be presented for parallel-summation logarithmic amplifiers. Such a design procedure is given in Section III, with proof of a logarithmic result. Some unique and efficient delay-matching structures are then given for these circuits to allow for ultrabroad band operation.

III. DESIGN PROCEDURE

A mathematical model of parallel-summation logarithmic amplifiers is presented here which may be used for design purposes. It will be proven that this method yields an exact logarithmic relationship between the output current and the input voltage of the amplifier at the breakpoints of the approximation.

Considering the parallel-summation logarithmic amplifiers in Figs. 5 and 6, the desired transfer function is shown in Fig. 7. The constant A is defined as the factor increase in the input voltage between the cusps of the logarithmic approximation. The current I_S is defined as the step in output current between the cusps of the approximation. The dynamic range of the logarithmic amplifier will be defined as A^N , so for a dynamic range D , the constant A is chosen as $D^{1/N}$.

The gains through the k_{th} paths in Figs. 5 and 6 are labeled as G_{pk} , where $k = 1, 2, \dots, N$. This is because the same signals are being generated in two different ways, using series and parallel amplifiers. For either topology, there are N discrete states corresponding to the cases where $N, N-1, \dots, 1$ paths are contributing linearly to the output current. A path ceases to contribute linearly once its output current limits at I_L . As the input voltage increases, the logarithmic structure passes through the N states where gain decreases and follows the series

$$\begin{aligned}
 G_N &= G_{p1} + G_{p2} + \dots + G_{pN} \\
 G_{N-1} &= G_{p1} + G_{p2} + \dots + G_{p(N-1)} \\
 &\dots \\
 G_k &= G_{p1} + G_{p2} + \dots + G_{pk} \\
 &\dots \\
 G_1 &= G_{p1}.
 \end{aligned} \tag{2}$$

These state gains are labeled on the right side of Fig. 7 at the signal levels at which they occur.

In any given state, the output current of the overall amplifier consists of two parts, the current that is proportional to the input voltage, and the fixed current supplied by the gain paths which have already limited. The output currents shown on the y axis of Fig. 7 may be expressed as a sum of these two components, as in

$$\begin{aligned}
 C &= V_{\min} G_N \\
 I_S + C &= A V_{\min} G_{N-1} + I_L \\
 2I_S + C &= A^2 V_{\min} G_{N-2} + 2I_L \\
 &\dots \\
 (N-k)I_S + C &= A^{N-k} V_{\min} G_k + (N-k)I_L \\
 &\dots \\
 (N-2)I_S + C &= A^{N-2} V_{\min} G_2 + (N-2)I_L \\
 (N-1)I_S + C &= A^{N-1} V_{\min} G_1 + (N-1)I_L \\
 NI_S + C &= V_{\min} G_N + NI_L.
 \end{aligned} \tag{3}$$

A straightforward solution to these equations may be found by allowing $I_S = I_L$. As well, since $G_1 = G_{p1}$ from (2), the overall amplifier gains G_k may be found from (3) by assuming that the gain of the lowest gain path G_{p1} is simply g_m , the gain of the first transconductance element. This yields the overall amplifier gains

$$\begin{aligned}
 G_1 &= g_m \\
 G_2 &= g_m A \\
 &\dots \\
 G_k &= g_m A^{k-1} \\
 &\dots \\
 G_{N-1} &= g_m A^{N-2} \\
 G_N &= g_m A^{N-1}.
 \end{aligned} \tag{4}$$

Using this knowledge of the gains in each state of the overall parallel-summation amplifier, the gains of the component amplifiers in both the progressive-compression and parallel-amplification structures may be derived.

Solving (2) and (4) yields the gains of the paths through the parallel-summation amplifiers

$$\begin{aligned}
 G_{p1} &= g_m \\
 G_{p2} &= g_m(A-1) \\
 G_{p3} &= g_m A(A-1) \\
 &\dots \\
 G_{pk} &= g_m A^{k-2}(A-1) \\
 &\dots \\
 G_{pN} &= g_m A^{N-2}(A-1).
 \end{aligned} \tag{5}$$

The path gains in (5) correspond directly to the amplifier gains in the parallel-amplification parallel-summation topology in Fig. 6, multiplied by the g_m of the transconductance elements. Note that these gains may be increased or decreased by any factor as long as their respective ratios stay the same.

Applying (4) to the progressive-compression topology, the gain of the first path is just g_m from the first transconductance element. The amplifier gains in Fig. 5 are

$$\begin{aligned}
 G_{A1} &= A-1 \\
 G_{A2} &= A \\
 &\dots \\
 G_{Ak-1} &= A \\
 &\dots \\
 G_{AN-1} &= A.
 \end{aligned} \tag{6}$$

In practice, it is more convenient in the progressive-compression structure to make the gain of amplifier G_{A1} equal to A so that all of the amplifiers are the same. This may be done provided that the first transconductance element is also scaled from gain g_m to $g_m A/(A-1)$.

Having chosen the gains, it may be shown that the breakpoints are logarithmically related to the input voltage. The proof bears some resemblance to the description of the linear-limit amplifier given in [7].

Assuming that the k_{th} path in Fig. 5 or 6 is just on the point of limiting, then the input is

$$V_{\text{in}k} = V_{\text{in}} = \frac{I_L}{G_{pk}}. \tag{7}$$

However, G_{pk} is known from (5) to be $G_{pk} = g_m A^{k-2}(A-1)$, so that

$$V_{\text{in}} = \frac{I_L}{g_m A^{k-2}(A-1)} \quad k \geq 2. \tag{8}$$

Additionally, if the k_{th} path is limiting, then there are $N-k$ paths with higher gains which are also limiting, and $k-1$ more paths which are still amplifying linearly. Thus, the output current is

$$I_{\text{out}} = (N-k)I_L + [G_{p1} + G_{p2} \dots + G_{pk}] V_{\text{in}}. \tag{9}$$

Using (2) and then (4)

$$G_k = G_{p1} + G_{p2} + \dots + G_{pk} = g_m A^{k-1}. \tag{10}$$

Substituting (8) and (10) into (9) yields

$$I_{\text{out}} = (N-k)I_L + \frac{A I_L}{A-1}. \tag{11}$$

Additionally, (8) is rewritten as

$$k = \log_A \left[\frac{A^2 I_L}{g_m V_{\text{in}}(A-1)} \right]. \tag{12}$$

Finally, substituting (12) into (11) gives

$$I_{\text{out}} = I_L \left[N + \frac{A}{A-1} + \log_A \left[\frac{g_m V_{\text{in}}(A-1)}{A^2 I_L} \right] \right] \tag{13}$$

which is the desired logarithmic relationship between I_{out} and V_{in} .

A check of (13) may be made by substituting values for V_{in} and verifying that the output current behaves as shown in Fig. 7. Consider the case where the k_{th} amplifier path is just on the point of limiting. The input voltage for this case is given in (8). Substituting this into (13) for V_{in} and simplifying gives

$$I_{\text{out}} = I_L \left[N - k + \frac{A}{A-1} \right]. \tag{14}$$

For different values of k , this equation evaluates to

$$\begin{aligned}
 k = N \quad I_o &= I_L \left[\frac{A}{A-1} \right] \\
 &= I_L \left[1 + \frac{1}{A-1} \right] \\
 k = N-1 \quad I_o &= I_L \left[1 + \frac{A}{A-1} \right] \\
 &= I_L \left[2 + \frac{1}{A-1} \right] \\
 &\dots \\
 k = 2 \quad I_o &= I_L \left[N-1 + \frac{1}{A-1} \right] \quad (15)
 \end{aligned}$$

which confirms that as each gain path limits, the output current increases by a fixed step as shown in Fig. 7. The constant C in Fig. 7 is identified from (15) to be $I_L/(A-1)$. As well, V_{\min} from Fig. 7 is identified from (3) as

$$V_{\min} = \frac{C}{G_N} = \frac{I_L}{(A-1)g_m A^{N-1}}. \quad (16)$$

There is one final consideration regarding the case of $k=1$ not considered in (8), which is the case where the lowest gain path limits. The highest output current considered in (15) is the case where the second lowest gain path, whose gain is $G_{p2} = g_m(A-1)$, limits and provides a current of I_L . The input voltage at this point is

$$V_{\text{in}} = \frac{I_L}{G_{p2}} = \frac{I_L}{g_m(A-1)}. \quad (17)$$

At this input voltage, the current provided by the lowest gain path is

$$I = g_m V_{\text{in}} = \frac{I_L}{A-1}. \quad (18)$$

This point occurs at the total system output current of $(N-1)I_S + C$ in Fig. 7, and in order for the logarithmic slope of the output to continue, the lowest gain path must provide another I_S of current before it limits. However, $I_S = I_L$, and so adding this to (18) yields

$$I_{L1} = \frac{I_L}{A-1} + I_L = \frac{A}{A-1} I_L \quad (19)$$

which represents the value of the limiting current required in the lowest gain path. Thus, the lowest gain path provides a maximum current that is $A/(A-1)$ times higher than the other paths.

A. Logarithmic Slope and Intercept

The response of logarithmic amplifiers may also be characterized in terms of the logarithmic slope and intercept of the transfer characteristic, as in

$$I_{\text{out}} = I_{\text{slope}} 20 \log_{10} \left(\frac{V_{\text{in}}}{V_{\text{intercept}}} \right). \quad (20)$$

The amplifier transfer function in (13) may be used to calculate these parameters for the given model. Solving (13) for the intercept yields

$$V_{\text{intercept}} = \frac{A^{(2-N-A/(A-1))} I_L}{g_m(A-1)}. \quad (21)$$

The logarithmic slope may be found from (13) to be

$$I_{\text{slope}} = \frac{dI_{\text{out}}}{d[20 \log_{10}(V_{\text{in}})]} = \frac{I_L}{20 \log_{10}(A)} \text{ A/dBv}. \quad (22)$$

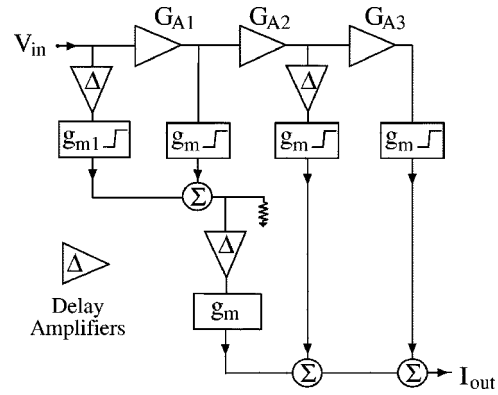


Fig. 8. Example of a three-stage delay-matched progressive-compression log amplifier.

Hence, the logarithmic slope is directly proportional to I_L and is inversely proportional to the logarithm of A .

B. Delay-Matched Progressive-Compression Amplifier

Having described a model of parallel-summation amplifiers, it is worth considering a disadvantage of the progressive-compression amplifier at high frequencies. In the progressive-compression circuit, the phase delays of each signal undergoing parallel summation will be different. This is because the first component signal in Fig. 5 does not pass through any amplifiers and has zero phase lag, and this signal must be added to the N th parallel signal, which will have significantly higher phase lag due to the output capacitance of each cascaded amplifier. A method proposed by the authors of extending the bandwidth is shown in Fig. 8, where the group delay and phase shift of each gain path are matched using delay amplifiers.² It has been recognized that the signals in the lowest gain paths may share delay amplifiers after they have been limited and summed. Any number of paths may be combined and delayed using this method, provided that the output voltage swing requirement of the shared delay amplifiers does not lower their bandwidth below that of the highest gain path.

IV. CIRCUIT DESIGN AND OPERATION

In this design, a novel hybrid series/parallel topology, as shown in Fig. 9, was chosen for implementation.³ A logarithmic voltage dynamic range of 50 dB was targeted, corresponding to a factor A of $320^{1/4} = 4.23$ in a four-branch amplifier. Thus, the scaled gains of the four paths are 1.00, 3.23, 13.7, and 57.8. However, in practice, some logarithmic dynamic range will be lost when dc coupling is used because the dc offsets in the component amplifiers will be amplified and will reduce the available signal swing.

The circuit uses cascode long-tail differential pairs, as shown in Fig. 10, for both the gain and delay amplifiers. The voltage outputs of the four amplification paths are each converted to currents and summed using the amplifier shown in Fig. 11. This summing/limiting circuit consists of four differential pairs in parallel. The circuit will sum an input signal up to the point

²Another solution was presented by Hughes in [14].

³Patent application pending.

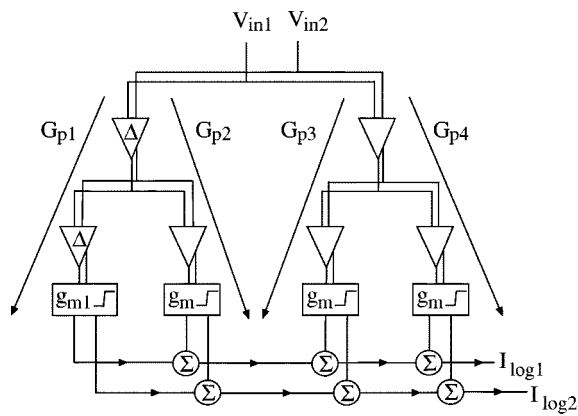


Fig. 9. Parallel-summation logarithmic amplifier implementation.

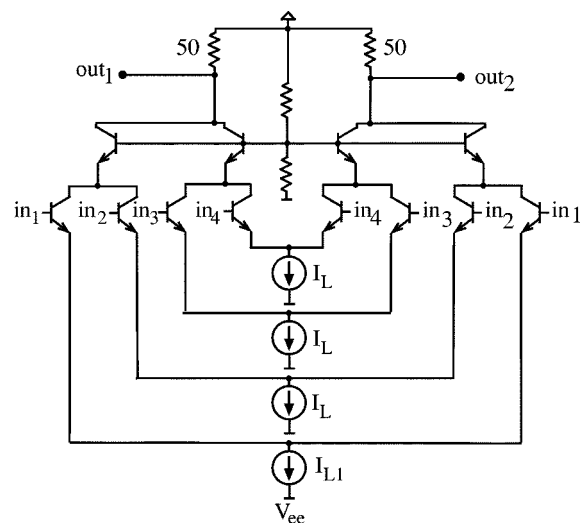


Fig. 11. Summing/limiting amplifier.

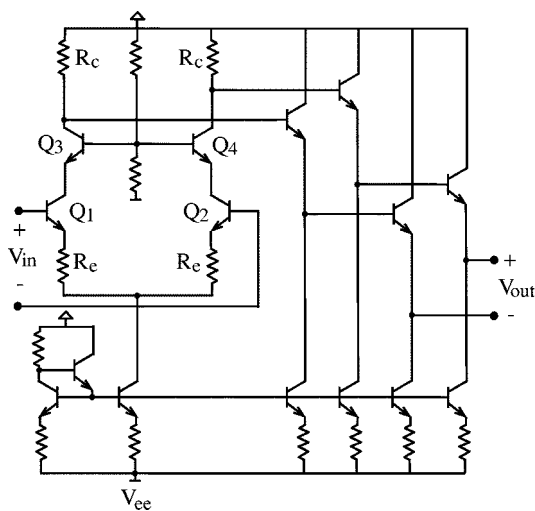


Fig. 10. Gain or delay amplifier.

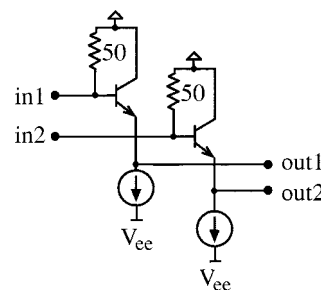


Fig. 12. Input matching circuit.

where that signal is large enough to steer all of the current in one of the differential pairs to one side, at which point it limits that input's contribution. The bias current in each amplifier in Fig. 11 is chosen as I_L , except the current in the lowest gain path, which is chosen as $I_{L1} = I_L A / (A - 1)$. This also increases the gain of that differential pair, however, the gain of the delay amplifiers in the lowest gain path may be lowered to compensate.

In addition to summing and limiting, the summing amplifier has a collector impedance of 50Ω , so as to allow for direct dc coupling of the output to a 50Ω system. The inputs of the chip are matched to 50Ω using the circuit shown in Fig. 12.

In this design, the technology used was a silicon bipolar process with an f_t of 35 GHz and a $0.35\text{-}\mu\text{m}$ minimum feature size. A die photograph of the $2 \times 2 \text{ mm}^2$ parallel logarithmic amplifier chip is shown in Fig. 13. It has a single supply voltage of -5 V and draws 150 mA of current. A negative supply voltage was used so that the circuit's input and output common-mode voltage would be close to zero.

The small-signal gain and reflection coefficients of the chip are shown in Fig. 14. The small-signal gain is 30 dB with a 3-dB bandwidth of 4.0 GHz. This is the highest bandwidth reported to date for a silicon true logarithmic amplifier, to our knowledge. The circuit is impedance matched at its input and output terminals within -10 dB for S_{11} and S_{22} up to 5 GHz.

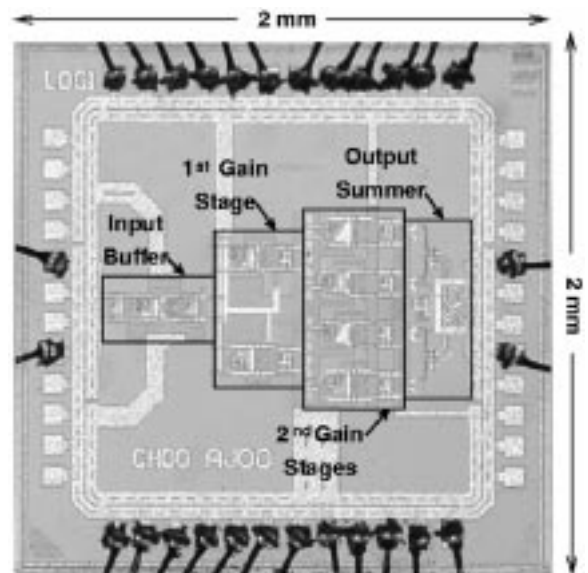


Fig. 13. Parallel logarithmic amplifier die photograph.

Variations in the group delay versus frequency are also of prime importance in the circuit's intended wide-band applications. Fig. 15 shows the measured small-signal group delay of the amplifier versus frequency. The maximum deviation of the group delay within the 4-GHz passband is 35 ps, which represents approximately one tenth of the period of a 2.5-Gb/s signal. The low group-delay distortion is a direct consequence of the

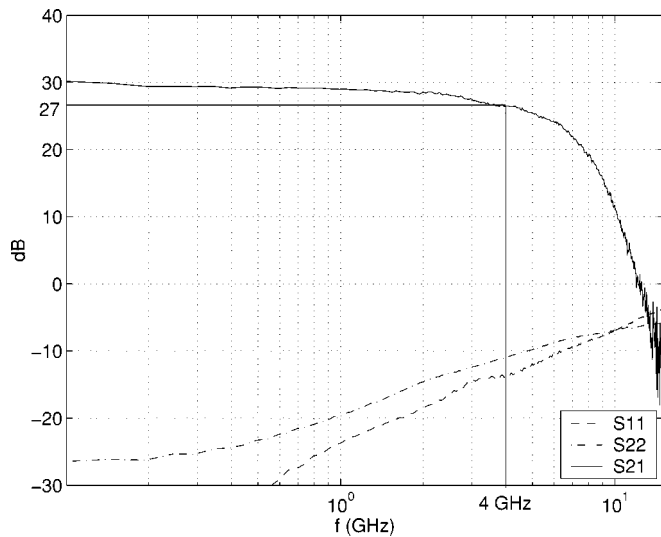


Fig. 14. Measured return loss and gain.

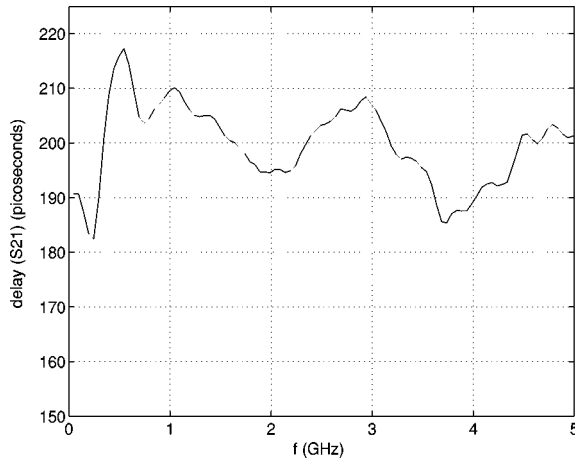
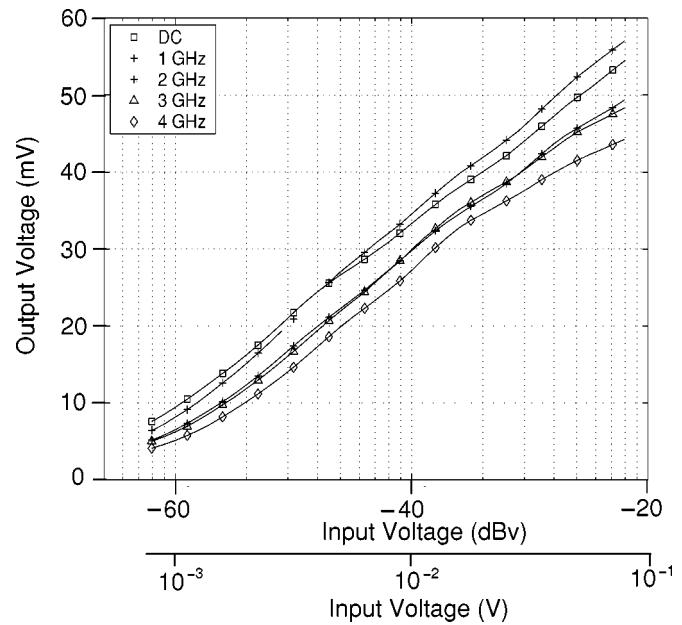


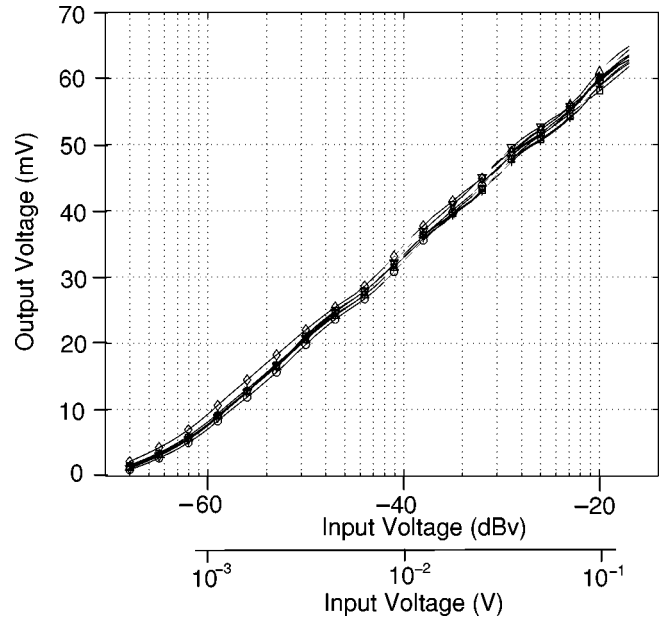
Fig. 15. Measured group-delay response.

parallel-summation topology used, which achieves low delay by using only two amplifiers in series to generate a four-segment logarithmic response.

The measured one-tone response of the chip is shown in Fig. 16(a) for frequencies from dc to 4 GHz. The single-ended logarithmic slope is approximately 1.2 mV/dB and the logarithmic intercept is 167 μ V. The slope could be increased in future implementations by increasing the bias currents in the circuit shown in Fig. 11. Regarding the effect of process variations on the logarithmic response, Fig. 16(b) shows the measured amplitude response of eight die samples at 1 GHz. The logarithmic slope is quite constant amongst the samples, indicating that the logarithmic response of the chosen topology may be designed to be robust. As a metric of logarithmic linearity, the logarithmic error was calculated for the responses in Fig. 16(a) at each frequency and also for a broad-band logarithmic fit. The definition of the log error is shown graphically in Fig. 3, where the definition of logarithmic error indicated in [1] and [15] has been used. This log error was computed at each 1-GHz interval, and is plotted in Fig. 17(a). It is seen that the log conformity is ± 2 dB over the 4-GHz interval. The



(a)



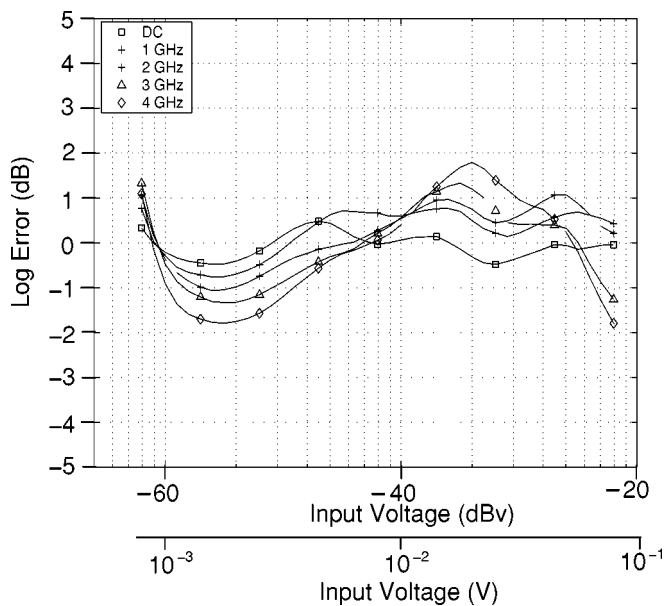
(b)

Fig. 16. Measured logarithmic responses. (a) Measured one-tone response at different frequencies. (b) Measured one-tone response at 1 GHz of eight die samples.

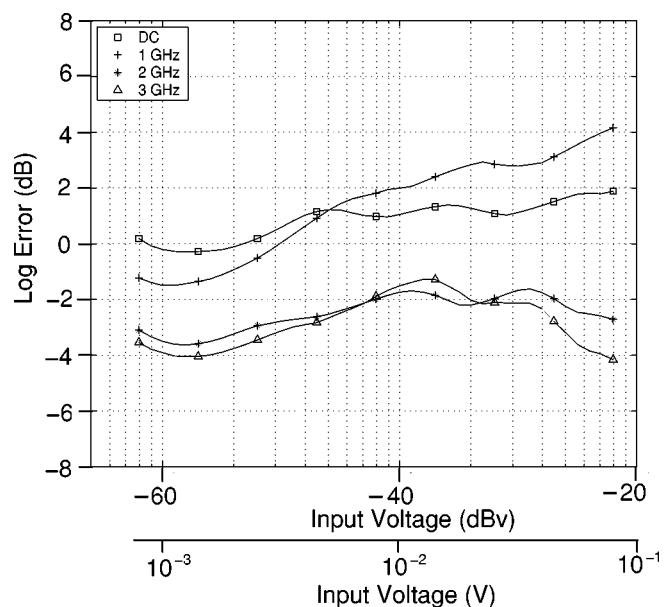
broad-band log error of the data fit to a single logarithmic line for a dc–3-GHz bandwidth is shown in Fig. 17(b), where the error is kept to a maximum of ± 5 dB.

Fig. 18 shows the normalized measured and ideal frequency-domain spectrum of the logarithmic amplifier output to a 1.8-GHz -10 -dBm signal with a 90-mV dc offset added in order to make the input signal greater than zero. The amplitude of the first three measured harmonics matches the ideal response well. The errors at the fundamental and first two harmonics are 0.5, 0.1, and 2.5 dB, respectively.

A real-time oscilloscope plot of the amplifier's response to a 40-dB range of input power at 1.8 GHz is shown in Fig. 19. The rise and fall times of this circuit are 100 ps each, the fastest



(a)



(b)

Fig. 17. Logarithmic error for separate and broad-band line fits. (a) Separate fit error. (b) Broad-band fit error.

reported to date for a microwave true logarithmic amplifier, to our knowledge.

In Fig. 19, it is apparent that the circuit contributes substantial noise for small signals, with the amount of noise decreasing as the higher gain-amplification paths begin to limit. The maximum input-referred noise density of the amplifier is $9 \text{ nV}/\sqrt{\text{Hz}}$. This corresponds to a maximum noise figure of 20 dB, which is undesirably high. Included in this version of the design was a unity-gain buffer at the input of the chip, which may be removed in future implementations. Another significant noise component in the logarithmic amplifier is the thermal noise arising from the parasitic base resistance of the transistors in Fig. 12, and from Q_1 and Q_2 in the first amplifier (see Fig. 10) in the highest gain path only. One method of

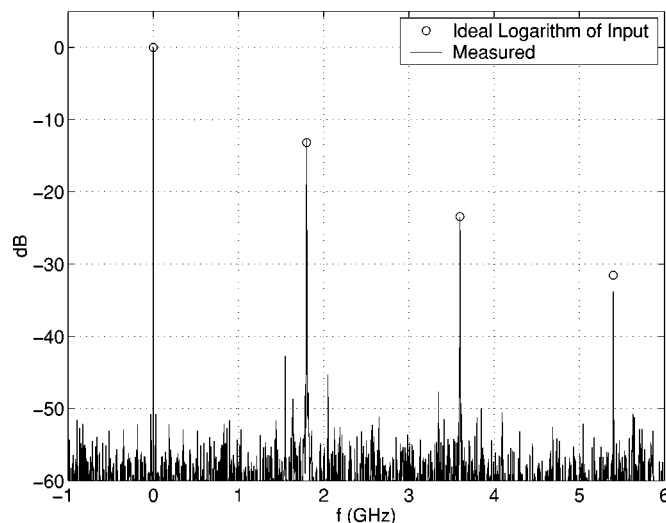


Fig. 18. Measured and ideal logarithmic amplifier output spectrum for a 1.8-GHz input tone.

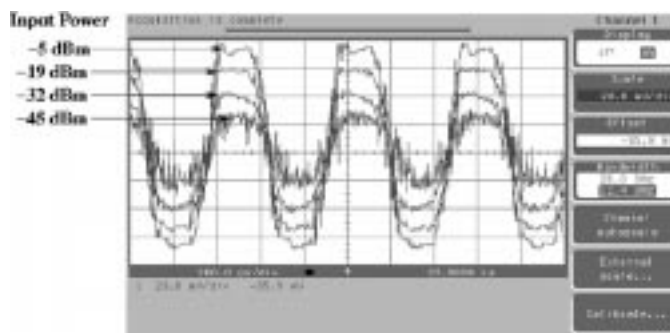


Fig. 19. Real-time oscilloscope plot of single-ended output voltage.

reducing this base resistance in future implementations is to use multiple transistors in parallel in these circuits [16].

In the real-time oscilloscope plot of Fig. 19, the log signal is also observed to peak or overshoot in response to the input sinusoid. In designing this chip, the delay through the two lower gain paths was set using delay amplifiers of the topology shown in Fig. 10. However, it was later determined that the delay of the buffer amplifiers could be increased to better match the high gain path. The resistive loads R_c interact with the parasitic capacitance of transistors Q_3 and Q_4 in the amplifier in Fig. 10 and form the dominant pole that limits the amplifier's bandwidth. The phase response of the delay amplifiers is approximately -45° near the pole frequency. The lower the dominant pole frequency, the more phase lag the amplifier contributes at lower frequencies. The derivative of the phase with respect to frequency defines the group delay, and so a lower 3-dB bandwidth corresponds to a higher group delay. Hence, amplifiers with increased group delay may be constructed by using differential amplifiers with sufficient capacitive loading to increase the delay as needed. The error in the phase shift through each gain path may be as high as approximately 20° at the log amplifier's highest frequency of operation without introducing significant distortion. Fig. 20 shows the simulated response of the amplifier with and without capacitive loading. It is seen that by including enough capacitance in the load of the

TABLE I
COMPARISON OF MICROWAVE TRUE LOG AMPLIFIERS

Circuit	Topology	Technology	Power Supply	Gain	Bandwidth	Rise/Fall Time	Dynamic Range	Log Slope
Acciari <i>et al.</i> [15]	Twin-Gain Stage	GaAs FET	-	36 dB	0.3-5 GHz	-	40 dB	10 mV/dB
Smith [18]	Twin-Gain Stage	GaAs FET Hybrid Circuit	-8V, +8V 5.2 W	70 dB	0.5-4 GHz	-	70 dB	6.3 mV/dB
Oki <i>et al.</i> [9]	Twin-Gain Stage	GaAs HBT	-8 V 1.06 W	48 dB	DC-3 GHz	400 ps/ 400 ps	40 dB	3.3 mV/dB $Z_o = 100\Omega$
This Work	Branch Parallel Summation	Silicon Bipolar $f_t = 35$ GHz	-5 V 0.75 W	30 dB	DC-4 GHz	100 ps/ 100 ps	40 dB	1.2 mV/dB $Z_o = 50\Omega$

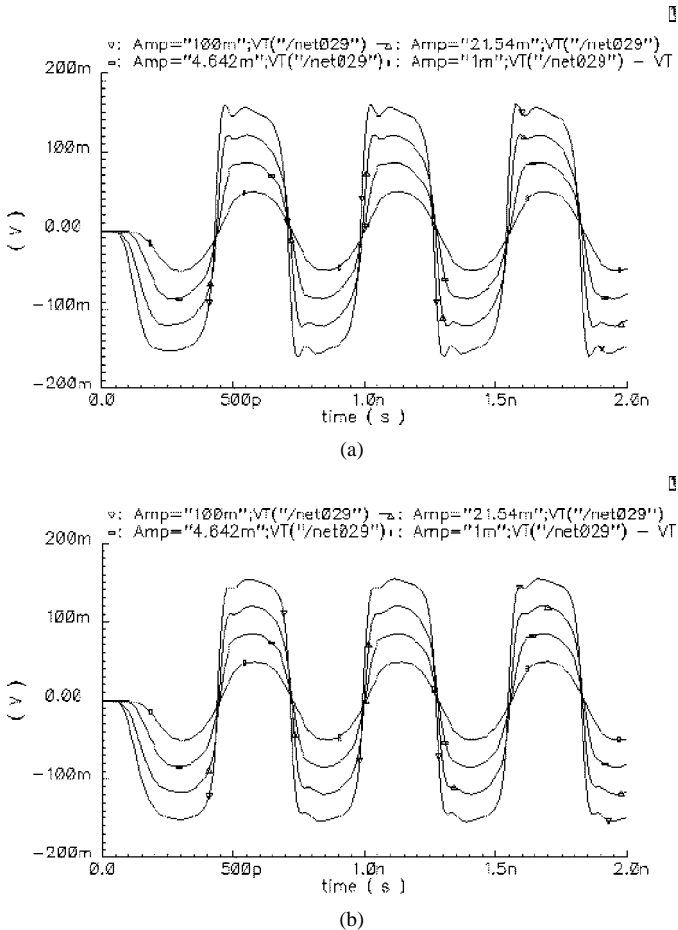


Fig. 20. Simulated log amplifier differential responses to sinusoidal inputs (a) without and (b) with capacitive delay tuning.

delay amplifiers, the response appears more like a compressed sinusoid, as desired. Care must be taken, however, not to lower the bandwidth of the delay amplifiers below that of the highest gain path.

Table I shows a comparison of this work with three other microwave true log amplifiers that are known to the authors. The bandwidth of this circuit is relatively high, showing that silicon logarithmic amplifiers are competitive with gallium-arsenide designs. The bandwidth of this circuit could be further increased through the use of parallel-feedback amplifiers (PFAs) instead of differential pairs as the building block of the log

amplifier [16], [17]. (PFAs are enhanced gain-bandwidth product differential pairs.) Furthermore, the circuits presented for this log amplifier are directly usable in silicon-germanium technologies, making further increases in the bandwidth achievable.

V. CONCLUSION

In this paper, a unified design procedure for parallel-summation logarithmic amplifiers which is proven to yield breakpoints on an exact logarithmic response was presented. A dc–4-GHz true logarithmic amplifier was constructed in a 35-GHz silicon bipolar process, making this the highest bandwidth silicon true logarithmic amplifier published to date. The amplifier uses a novel hybrid series/parallel-amplification topology, resulting in a maximum group-delay variation of 35 ps within the passband. The log amplifier topology is well suited for baseband operation in fiber-optic networks.

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