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Two Baseband Logarithmic Amplifier Designs Using Parallel Feedback Amplifier Cells

Chris D. Holdenried and James W. Haslett *

Abstract

In this work, parallel feedback amplifiers (PFAs) are presented as a means of generating ultra broadband logarithmic amplifiers. The low frequency gain equations and an AC model of PFAs are given. A circuit is presented for automatic, on-chip DC offset error reduction. In addition, circuits for achieving temperature and process stable, high power, low noise logarithmic amplifiers are described. The performance simulations of a DC - 7.5 GHz logarithmic amplifier are described. The circuit has been submitted for fabrication in a 47 GHz f_t silicon germanium BiCMOS process. The integrated circuit occupies 2 mm², consumes 667 mW of power from a -3.3 V supply, has 42 dB of logarithmic dynamic range, 50 ps rise/fall times, and a 12 mV/dB single ended logarithmic slope.

1 Introduction

Logarithmic amplifiers are widely used in applications involving high dynamic range analog data. They are primarily used in receivers for radar and radio. Radio signals may fade during transmission, causing the received power to fluctuate by many tens of decibels. Logarithmic amplifiers compress the dynamic range of a signal because their gain decreases as the signal amplitude increases. Other applications of logarithmic amplifiers are in instrumentation requiring the logarithmic operation, and in conditioning sensor outputs.

A new application of logarithmic amplifiers is in the generation of optical single sideband signals [1, 2, 3, 4]. In this application, the logarithmic amplifier must have rise and fall times which are less than the

period of the data being transmitted. This requirement is similar to that of radar applications that use narrow pulse widths. Not only must the logarithmic amplifier have short rise and fall times, but the group delay throughout the passband of the logarithmic amplifier must be reasonably constant in order to prevent pulse distortion. Furthermore, the logarithmic amplifiers of particular interest in this work must operate at baseband, although they may also operate directly on a bandpass IF or RF signal. To allow for baseband operation, the amplifiers must be DC coupled throughout. Unfortunately, high gain DC coupled differential amplifiers may have large DC offset errors which can greatly reduce the available voltage swing within the amplifier. To address this issue, an on-chip DC offset reduction scheme is presented in this work.

It is critical with any logarithmic amplifier design that the output noise be minimized through careful design. In the present work, multi-gigaHertz bandwidth amplifiers are considered. In such a circuit, the noise at all frequencies adds in the time domain to create a relatively large noise signal. The amplitude of the input referred time domain noise of a logarithmic amplifier imposes a lower bound on the input signal amplitude which may be sensed reliably. The two amplifiers in this work were carefully designed to be low noise, as will be described.

The magnitude of the logarithmic amplifier output signal is characterized in terms of logarithmic slope, defined as the change in output signal amplitude in response to some factor increase in the input signal amplitude [1, 5]. In this work, an amplifier which features high logarithmic slope and relatively low power consumption is described.

In addition to the aforementioned considerations, logarithmic amplifiers must provide reliable operation despite variations in process and temperature. The two logarithmic amplifiers in this work contain several features to ensure reliable operation, as will be described.

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C. Holdenried and J. Haslett are with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, Alberta, Canada T2N 1N4, and also with TRILabs, Calgary, Alberta, Canada T2L 2K7 (e-mail: holdenri@cal.trilabs.ca; haslett@enel.ucalgary.ca).

2 Circuit Design

Given the challenge of designing a multi-gigaHertz bandwidth logarithmic amplifier, it is too difficult to realize an exact logarithmic response. Hence, piecewise approximate logarithmic amplifiers are used in this work. The error introduced in the output signal by the piecewise approximate response is less than 1 dB in most of cases.

The first true logarithmic amplifier design is shown in Fig. 2 a). This design is based on the parallel summation architecture, and uses a hybrid series/parallel topology. There are four gain paths each terminating in a limiting transconductance element. The highest gain path, G_{p4} , consists of two series amplifiers, each of which are surrounded by a feedback amplifier which is used to reduce their DC offset errors. Compared to AC coupling of the amplifiers, this scheme greatly reduces the high pass corner frequency of the amplifier. Therefore, it may be used in RF carrier applications and also in multi-gigaHertz baseband transmission systems.

The four different amplification paths in Fig 2 a), $G_{p1} - G_{p4}$, will successively cause the transconductance elements to limit their output current in response to an increasing input signal amplitude. The output currents of all of the transconductance elements are summed to form the logarithmic output signal. The amplifier's response is shown in Fig. 1, and it approximates a straight line when plotted on a semilogarithmic axis. A key advantage of this structure is that the limiting of the signals is performed at the output of the amplifier and so the limited signals do not need to be delayed. This gives the designer the freedom to design for a large logarithmic slope. To choose the gain of each amplification path to yield a logarithmic response, the design procedure in [1] was used.

The second logarithmic amplifier design in this work uses the well known series linear-limit topology, as shown in Fig. 2 b). The forward path of the linear-limit amplifier consists of a cascade of dual gain cells, with each cell having a high gain limiting amplifier in parallel with a unity gain buffer. This circuit is further described in [1, 5]. It's response is the same as design 1, and is also shown in Fig. 1. The more stages that are cascaded in the linear-limit amplifier, the higher the gain and dynamic range which may be achieved. However, this high gain combined with any asymmetry in the components in the first few stages of the amplifier will generate large DC offset errors. These errors will be amplified by the later stages in the amplifier and may easily be large enough to cause the high gain amplifiers in the later stages to limit,

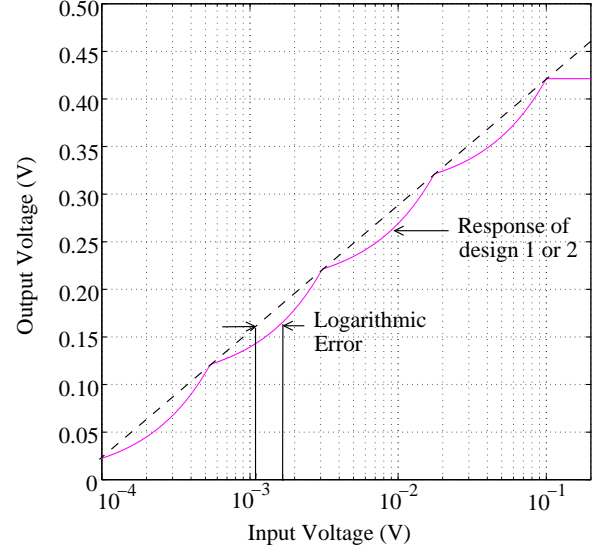


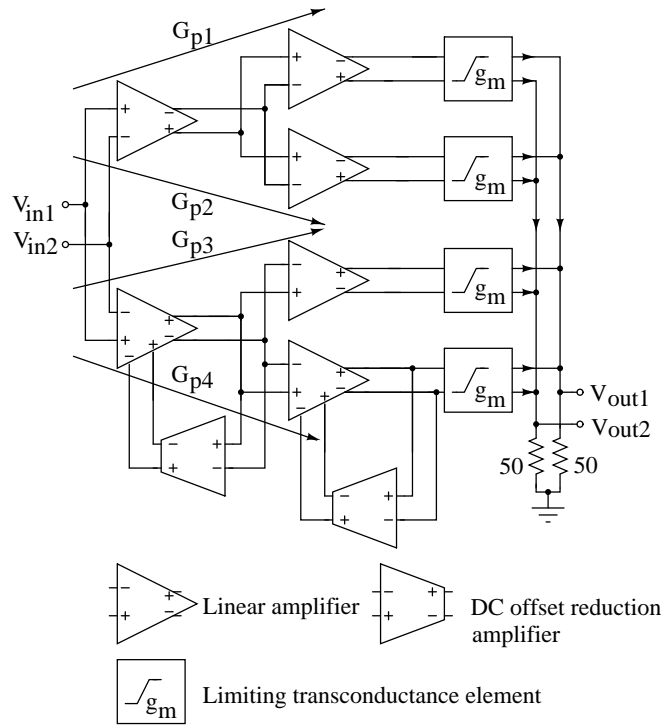
Figure 1: Ideal logarithmic amplifier transfer functions

thereby reducing the logarithmic dynamic range. For this reason, this design also includes an automatic DC offset error reduction scheme. Surrounding each of the first two stages of the linear-limit amplifier are DC-2 MHz amplifiers which are connected in negative feedback around the stages in order to suppress DC offset errors.

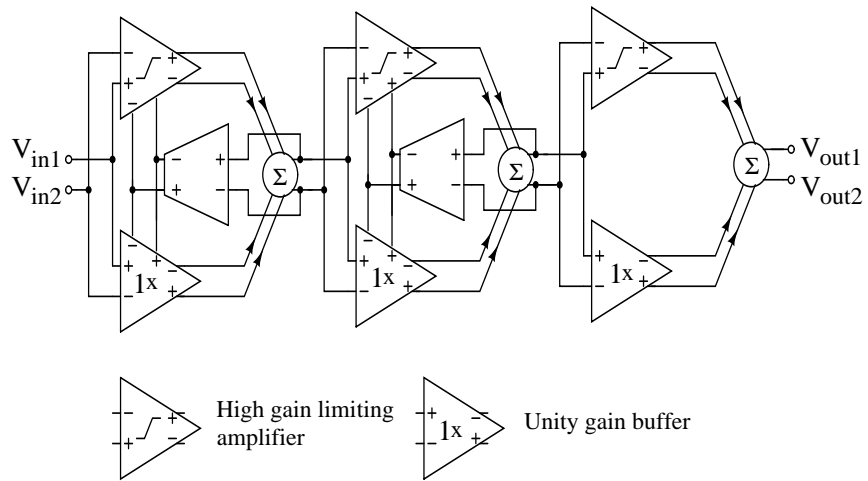
2.1 Traditional Implementations

The most common implementation of one of the twin gain stages of the series linear-limit logarithmic amplifier consists of two differential pairs in parallel, as shown in Fig. 3 [5, 6, 7]. Both amplifiers share the same load resistor R_c so that their output currents are summed across this resistor. The unity gain buffer contains resistive emitter degeneration to provide low gain, and the high gain limiting amplifier is undegenerated to provide high gain. It is desired that the unity gain buffers in each stage continue to pass the signal until all of the high gain amplifiers have limited. For this reason, it may be shown that I_{low} must be made at least as large as kI_{high} , where k is the number of the stage.

The bandwidth of one of these stages is typically determined by a pole which is the result of the load resistor R_c interacting with the parasitic capacitance at the collector node of the four transistors. A series linear-limit amplifier consists of multiple stages, and so the bandwidth of the overall amplifier rolls off



(a) Design 1: Parallel summation logarithmic amplifier



(b) Design 2: Series linear-limit logarithmic amplifier

Figure 2: True logarithmic amplifier designs

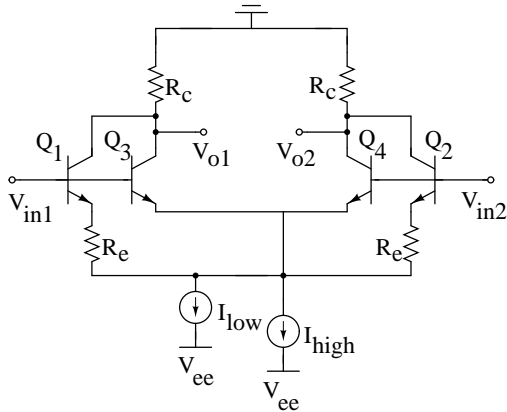


Figure 3: High gain limiter and unity gain buffer parallel

faster with frequency than the bandwidth of one of the stages. This makes it difficult to achieve bandwidths with the series linear-limit logarithmic amplifier that are comparable to the bandwidths of parallel summation logarithmic amplifiers, such as the design shown in Fig. 2 a). This is unfortunate, since the series linear-limit topology provides an elegant means of logarithmic amplification. In this work, a novel twin gain stage implementation is presented which greatly improves the frequency response of the series linear-limit amplifier over the traditional implementation.

The traditional twin gain stage implementation in Fig. 3 uses differential pairs. Differential pairs are also used in an implementation of a parallel summation logarithmic amplifier presented by the authors [1]. However, in recent years, the Parallel Feedback Amplifier (PFA) has emerged as a gain cell that may be used in place of the differential pair [8, 9, 10]. The PFA is an enhanced gain-bandwidth product differential pair, and has found application in receivers for fiber-optic networks. In the next section, the use of the PFA in logarithmic amplifiers is presented (patent applied for).

2.2 Description of PFA Gain Stages

The schematic diagram of a PFA is shown in Fig. 4. The basic PFA consists of two differential pairs in series, with the output of the second stage fed back to the output of the first stage. The circuit in Fig. 4 also shows, in dotted lines, the necessary additions to make it a twin gain PFA.

The principle of the PFA's improved frequency response is that its transfer function contains a zero

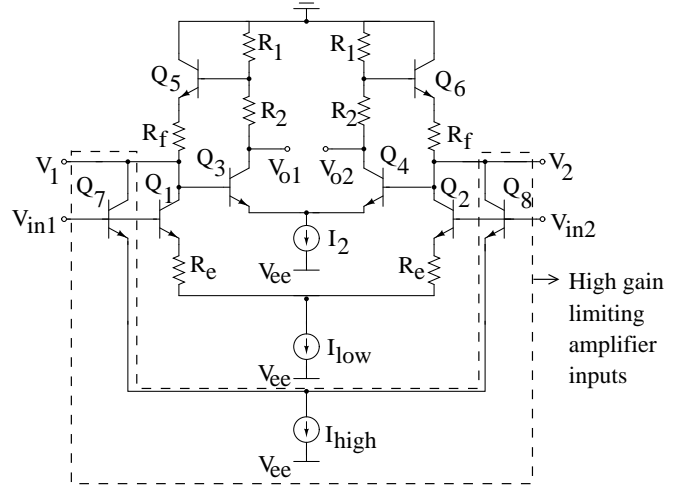


Figure 4: Basic PFA and twin gain PFA

which allows the gain to be constant out to higher frequencies. However, before investigating the AC performance of these cells, the DC gain equations will be given. The DC gain of the basic PFA in Fig. 4 is approximately given by

$$G_{PFA} \cong \frac{(R_f + r_{d5})(R_1 + R_2)}{(r_{d1} + R_e)(R_1 + r_{d3})} \quad (1)$$

where r_{d1} , r_{d3} , and r_{d5} are the inverse of the transconductance of transistors $Q_{1,2}$, $Q_{3,4}$ and $Q_{5,6}$ respectively. The implications of using resistor R_e in Fig. 4 are explored in Section 2.3.

The gain of the high gain limiting amplifier, which includes Q_7 and Q_8 , is approximately given by

$$G_{high} \cong \frac{g_{m1}(R_f + r_{d5})(R_1 + R_2)}{(R_1 + r_{d3})}. \quad (2)$$

In the case where this high gain path is added, the resulting twin gain stage will be one of numerous cascaded amplifiers in the series linear-limit amplifier in Fig. 2 b). Similar to the traditional linear-limit implementation, it is desired that the low gain path continue to buffer the signal while the high gain paths in each stage limit. For this reason, the limiting level of the unity gain buffer must be k times higher than the limiting level of the high gain amplifier in the k^{th} stage. Currently, research is under way on how to best design the twin-gain PFA to achieve this large signal response. Such a design should be possible, and would greatly improve the frequency response of the traditional twin gain stage.

A key advantage of PFAs is their superior frequency response. The important parasitic elements

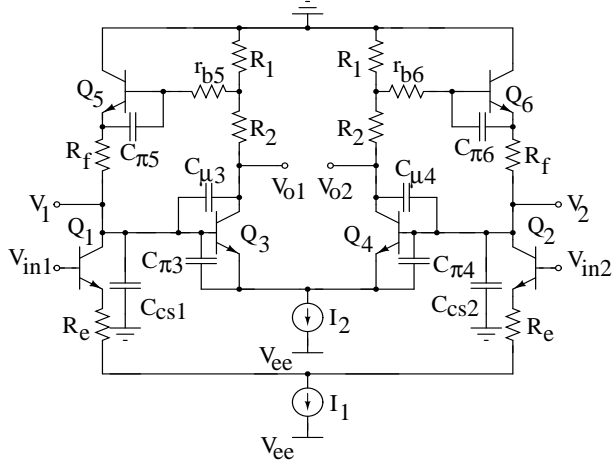


Figure 5: Parallel feedback amplifier small signal circuit

of a PFA will now be identified. In the PFA in Fig. 4, each of $Q_1 \rightarrow Q_6$ will have a parasitic collector to substrate capacitance C_{cs} , base to emitter capacitance C_π , and base to collector capacitance C_μ . However, for modern integrated bipolar transistors, $C_\pi \gg C_{cs}, C_\mu$. In addition, it is assumed that the circuit is being driven at the input with a low impedance source, so that the pole at the input of the circuit created by C_π of Q_1 and Q_2 is at very high frequency and may be neglected. Using these simplifications, the small signal circuit reduces to that shown in Fig. 5, where the transistors shown have no parasitics other than those which are shown explicitly. The parasitic resistors r_{b5} and r_{b6} are on the order of magnitude of R_1 , R_2 , and R_f and so are included for improved accuracy. A number of simplifications to this circuit are possible. It is recognized that the emitter node of Q_3 and Q_4 forms a virtual small signal ground, and so $C_{\pi 3}$ may be added to C_{cs1} and $C_{\pi 4}$ may be added to C_{cs2} . Furthermore, $C_{\mu 3}$ and $C_{\mu 4}$ may be added to these capacitances as well if they are reflected to nodes V_1 and V_2 using Miller's theorem with the gain across $C_{\mu 3,4}$. Miller's theorem also indicates that $C_{\mu 3,4}$ will be reflected to nodes V_{o1} and V_{o2} , but the pole created at these nodes will be at a much higher frequency and may be ignored. Note that this assumption does not hold when MOS transistors are used, because the junction capacitance at the drain of an NMOS transistor is quite large. The resulting small signal circuit has just two pairs of capacitors, $C_{\pi 5}$ and $C_{\pi 6}$ as well as a capacitance to ground at nodes V_1 and V_2 .

The frequency response of a simple differential pair

is dominated by a single low frequency pole, and so the addition of a zero makes the PFA capable of improved AC performance. Furthermore, since the PFA gain may be more or less constant out to a high frequency, the overall bandwidth of multiple cascaded PFAs also tends to be flat. This is in contrast to the gain of multiple cascaded differential pairs, which tends to roll off quickly with increasing frequency.

2.3 Noise performance of the PFA

In Fig. 4, degeneration resistor R_e is included in the basic PFA. The reason for using resistor R_e may be seen by examining what happens when R_e is omitted. If it assumed that $R_e = 0$, and that R_1, R_2 , and $R_f \gg r_{d1}, r_{d3}$, and r_{d5} , then equation (1) reduces to

$$G_{PFA} \cong \frac{g_{m1} R_f (R_1 + R_2)}{R_1}. \quad (3)$$

Although a precise value of $(R_1 + R_2)/R_1$ may be set using resistive matching, the value of R_f may change by as much as 30%. If R_e is included, then the gain becomes dependent on $R_f/(R_e + r_{d1})$ which may be more precisely controlled. However, using resistor R_e is undesirable for two main reasons. When designing a PFA, since R_e appears in the denominator of equation (1), an increased R_f is required to achieve high gain and a good frequency response. However, larger resistances increase the time constants within the amplifier, and lower the bandwidth. As well, R_e generates thermal noise, the voltage gain of which to the PFA output is given by equation (1). For these reasons, it would be desirable if R_e could be omitted.

Fig. 6 shows the PFA without R_e and with a Widlar-type current source for I_1 with a β -helper transistor. The benefit of this bias configuration will now be explained. It is assumed that $\beta_f \gg 1$ for the transistors, where $\beta_f = I_C/I_B$ and I_B and I_C are the base and collector DC currents for a given transistor. The output current I_1 of this mirror is given by

$$I_1 \cong \frac{V_T}{R_{m2}} \ln \left(\frac{I_1 I_{sm2}}{I_{ref} I_{sm1}} \right) \quad (4)$$

where I_{sm1} and I_{sm2} are the scaling currents of Q_{m1} and Q_{m2} respectively. This shows that I_1 is proportional to absolute temperature (PTAT), because it is dependent on $V_T (= kT/q)$ where k is Boltzmann's constant, T is absolute temperature, and q is the electron charge. Furthermore, the larger the ratio I_{sm2}/I_{sm1} and hence the ratio of emitter lengths of Q_{m2} to Q_{m1} , the larger the current I_1 and the more steeply it increases with increasing temperature. Half of I_1 is the quiescent bias current of Q_1 or Q_2 . Hence the transconductance of these transistors becomes

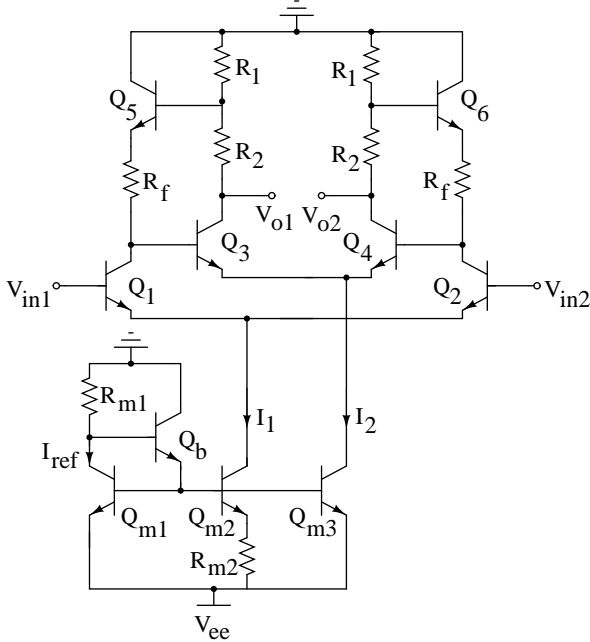


Figure 6: PFA with PTAT current biasing

$$g_{m1,2} = \frac{I_{c1,2}}{2V_T} \cong \frac{1}{2R_{m2}} \ln \left(\frac{I_1 I_{s2}}{I_{ref} I_{s1}} \right). \quad (5)$$

Using this, the PFA gain in equation (3) becomes

$$G_{PFA} \cong \frac{R_f(R_1 + R_2)}{2R_{m2}R_1} \ln \left(\frac{I_1 I_{s2}}{I_2 I_{s1}} \right). \quad (6)$$

The significance of this equation is twofold. It is evident that the gain is no longer directly proportional to temperature, since the PTAT current source counteracts the inverse dependence of g_{m1} and g_{m2} on temperature. Furthermore, G_{PFA} is only dependent on the ratios $(R_1 + R_2)/R_2$ and R_f/R_{m2} , both of which may be set accurately despite variations in process. In the present designs, all of the undegenerated emitter-coupled pairs at the PFA inputs are biased using this scheme. This improves both the frequency response and the noise performance of the amplifiers compared to the case where the emitter-coupled pairs are degenerated with R_e , all while maintaining temperature and process stability of gain.

2.4 DC offset error reduction circuits

Figs. 7 shows the schematic diagram of the first amplifier in the highest gain path in design 1, along with its input buffer and DC offset reduction amplifier. The BiCMOS offset reduction amplifiers are

used only in the highest gain path. The offset reduction amplifier consist of a SiGe HBT emitter coupled pair with PMOS active loads. This configuration provides a very high impedance node which is loaded with a 4 pF capacitor in order limit the feedback bandwidth to 2 MHz. It may be shown that if the gain of the feedback amplifier is much higher than that of the main amplifier, and if the feedback is negative, then the output referred DC offset error of the main amplifier will be reduced to the input referred DC offset error of the feedback amplifier. This prevents the DC offset errors in the highest gain path from drifting to undesirable levels. Furthermore, the DC error reduction amplifiers may be switched on or off by connecting the supply voltage of their current bias to the circuit's positive or negative voltage supply.

Also included in Fig. 7 is the input buffer. A negative supply voltage is used, and the input of each circuit contains an emitter follower with a resistive divider at the input. This divider is used to lower the input common mode voltage level and to set the input impedance to 50 Ω . The transistors in the input emitter followers and at the input of the PFA each have a multiplicity of 2. Multiple transistors are used in order to lower the base resistance and hence the thermal noise arising from this resistance [8].

Fig. 8 shows the summing/limiting circuit of design 1, which consists of four differential pairs in parallel. This circuit limits each path signal when that signal is large enough to steer all of one of the differential pair currents to one side. Furthermore, each differential pair in the output summing circuit is biased with a very large current, 12 mA, in order to create a very large logarithmic slope. The lowest gain path is biased with 16 mA for improved logarithmic accuracy [1]. The high currents in the output summing circuit would normally give it a very high gain, except that it uses emitter degeneration in order to keep the gain at approximately 1.5. This gain is low enough not to amplify DC offset errors, but is not so low as to make it difficult to cause the summer branches to limit. The input common mode voltage of the summing amplifier is lowered to a convenient level using Schottky diodes which are bypassed by a 600 fF capacitor. There are a total of four gain paths in design 1, and it is necessary to make sure that the phase shift through each path is roughly the same throughout the bandwidth of operation. The error in the phase shift through each path is less than 20° at all frequencies within the passband.

For design 2, the first twin gain stage would be similar to that shown in Fig. 7, except that a twin gain PFA would be used in place of the basic PFA.

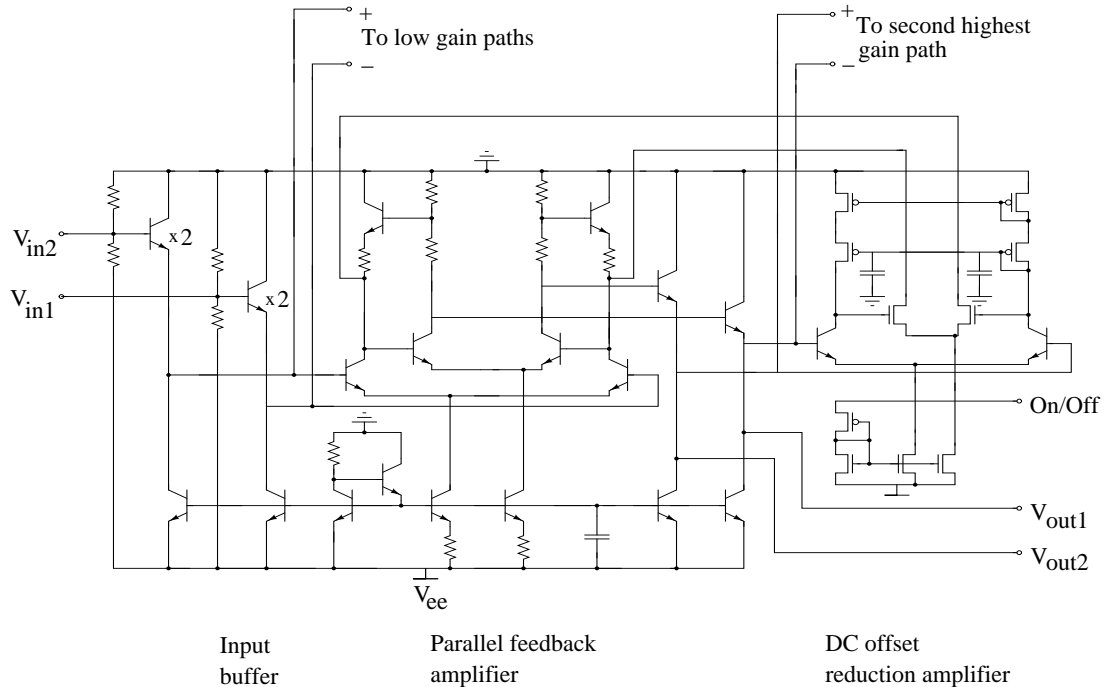


Figure 7: Schematic diagram of the input buffer, first amplifier in the highest gain path, and DC feedback amplifier for design 1

For the last twin-gain PFA stage, it is important to know the output impedance. This is so that it could be designed as 50Ω to allow for direct connection to microwave systems. The output impedance of a PFA in Fig. 4 is given approximately by

$$R_{out} \cong \frac{(R_1 + 2r_{d3})(R_1 + R_2)}{2(R_1 + r_{d3})}. \quad (7)$$

For $R_1, R_2 \gg r_{d3}$, R_{out} reduces to $(R_1 + R_2)/2$. Hence, large resistor values may be used to maintain a high gain without significantly increasing the impedance.

3 Performance Simulations

Figs. 9 shows a die plot of an implementation of design 1 which has been submitted for fabrication. The circuit occupies $1.4 \times 1.4 \text{ mm}$ which is approximately 2 mm^2 . The technology used is a 47 GHz f_t silicon germanium BiCMOS process with $0.5 \mu\text{m}$ gate width CMOS transistors available. The circuit consumes 202 mA from a single -3.3 V supply. The power consumption of each subcircuit is labeled on the die plot. The DC offset error reduction amplifiers consume negligible power. A large part of the power con-

sumption of the circuit is concentrated in the output summing/limiting circuit in order to achieve a high logarithmic slope. The input buffer also consumes a large amount of power. The currents of the input emitter followers were designed to minimize the emitter current shot noise and base resistance thermal noise of the transistors.

Fig. 10 shows the small signal response of the circuit. The gain is 29.4 dB at DC, increases to 33.5 dB at 10.0 GHz, and decreases to 26.4 dB at 10.8 GHz. The value of S_{11} is less than -10 dB from DC to 8.5 GHz and is -6.5 dB at 10 GHz. These simulated performance parameters include the effect of extracted parasitic capacitances. Also shown in Fig. 10 is the magnitude response for the case where the DC offset reduction amplifiers are turned on. In this case, each amplifier has a high pass corner frequency of 2 MHz, and DC signals are suppressed in the highest gain path.

Fig. 11 shows the one tone amplitude response of the design for a number of frequencies. The design maintains a logarithmic characteristic up to 7.5 GHz, beyond which the response rolls off. This bandwidth is 50% higher than the previous best published true log amplifier bandwidth, which is 5 GHz to our knowledge [11]. The logarithmic slope of the transfer char-

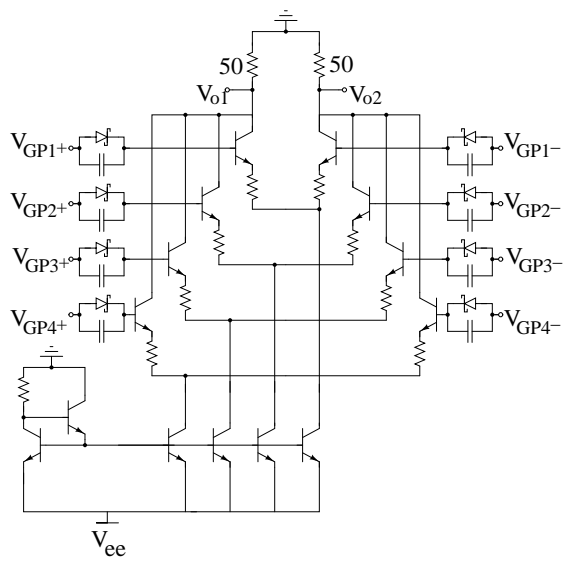


Figure 8: Summing/limiting circuit

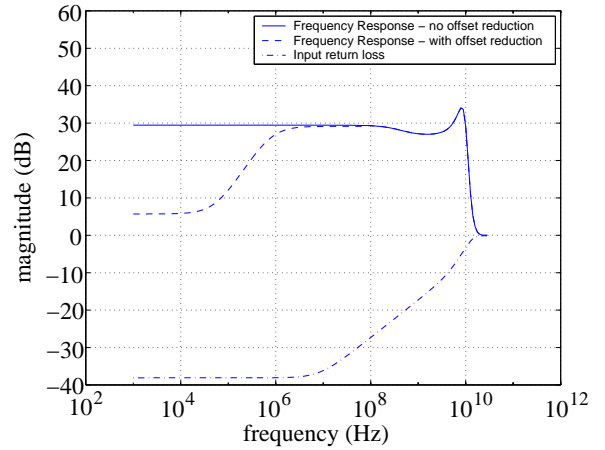


Figure 10: Simulated small signal gain and return loss of design 1

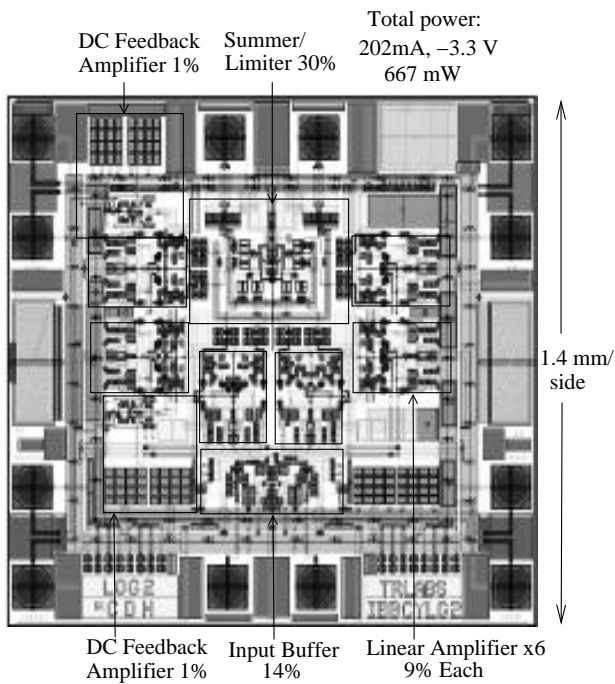


Figure 9: Die plot and power consumption of design 1

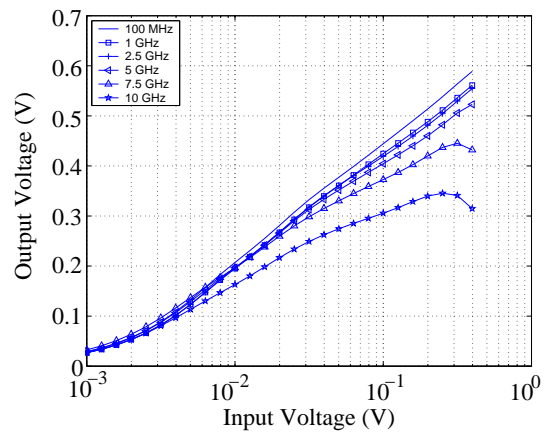


Figure 11: One tone amplitude response of design 1 at different frequencies

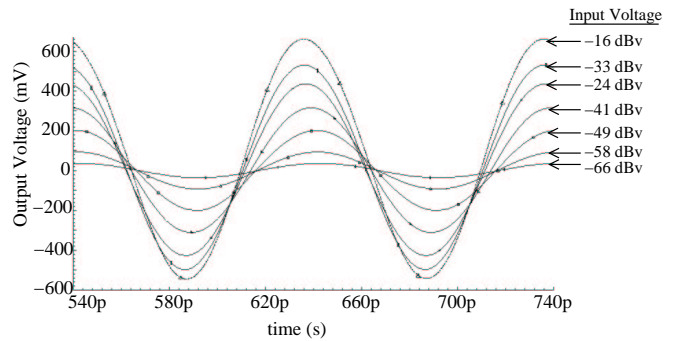


Figure 12: Transient responses of design 1 at 10 GHz

acteristic is 12 mV/dB over a 42 dB range. This is also higher than the previous best published multi-gigaHertz true log amplifier performance, which is 10 mV/dB [12].

The error in the logarithmic response was calculated for both single frequency curve fits and a broadband curve fit. The definition of logarithmic error is shown graphically in Fig. 1. The individual frequency logarithmic linearity is within ± 2.5 dB between input signal levels of 3 mV and 400 mV up to 7.5 GHz, corresponding to 42 dB of signal range. The broadband logarithmic linearity is within ± 3 dB for signal levels of 3 mV to 300 mV for frequencies up to 5 GHz.

The transient response of the design to a 50 dB range of input voltage levels at 10 GHz is shown in Fig. 12. The logarithmic amplifier compresses this dynamic range to less than a decade, as shown. The high logarithmic slope yields a high power, 1 V_{pp} output signal. This is despite the fact that the rise and fall times are 50 ps, half of that reported for any previous multi-gigaHertz true log amplifier, to our knowledge.

The total input referred noise of the circuit, integrated from 10 Hz to 20 GHz, is 213 μ V. This is comparable to the input referred noise of 275 μ V reported by Greshishchev and Schvan for a low noise 10 Gb/s limiting amplifier for a fiber optic receiver front end [8].

4 Conclusions

The design of low noise, temperature and process stable PFAs and true logarithmic amplifiers was presented. A topology for a novel, twin gain logarithmic amplifier stage was described, which may greatly improve the frequency response of the linear-limit logarithmic amplifier. A BiCMOS DC-7.5 GHz true logarithmic amplifier was described. The integrated circuit occupies 2 mm² and consumes 667 mW from a single -3.3 V supply. The circuit includes an automatic, on-chip DC offset error reduction scheme.

5 Acknowledgment

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