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Modified CMOS Cherry-Hooper Amplifiers with Source Follower Feedback in 0.35 μm Technology

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Abstract

A CMOS Cherry-Hooper amplifier that is modified to include source follower feedback is described. A small signal model that uses only the most dominant capacitances is used to derive the transfer function of the circuit. The gain is significantly higher than that of the standard MOS Cherry-Hooper stage. Design techniques based on the analysis are suggested for broadband applications.

A test circuit, fabricated in a 0.35 μm CMOS technology, has 9.4 dB gain and 880 MHz bandwidth while consuming 6.0 mA from a 3.3 V supply. Eye diagrams of the test chip at 630 MS/s show good eye opening, giving confidence to the new amplifier's large signal performance.

In addition, a six stage main amplifier using the modified Cherry-Hooper stages was fabricated in a 0.18 μm CMOS technology. It draws 44 mA from a 1.8V supply. It has 39 dB single-ended gain, 2.1 GHz bandwidth, and 14.2 dB noise figure.

1. Introduction

The low transconductance of MOS transistors compared to bipolar devices presents a significant challenge to the designer of CMOS receivers for optical applications. One choice for the design of CMOS main amplifier (MA) stages is the Cherry-Hooper amplifier [1]. These amplifiers provide a high gain-bandwidth product without the extra supply voltage or chip area needed for inductively peaked gain stages with active or passive inductors.

This paper introduces MOS Cherry-Hooper amplifiers with source-follower feedback and an additional feedback resistor for enhanced gain. The dominant capacitances in these amplifiers are identified. Equations and models describing the small signal AC performance are given. The small and large signal performances are then demonstrated using measurements of a test amplifier in a 0.35 μm CMOS technology.

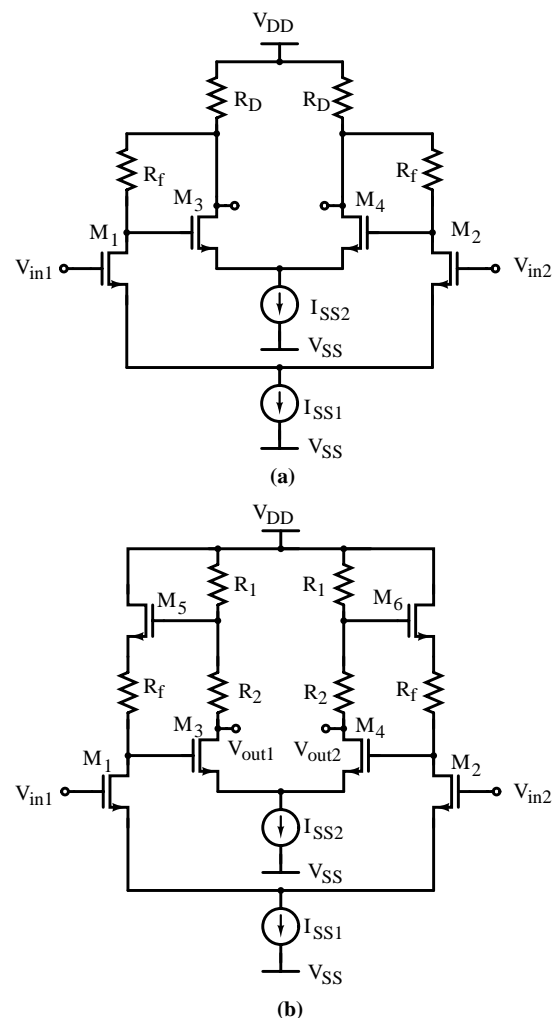


Figure 1. MOS Cherry-Hooper amplifier a) standard form b) modified form with source follower feedback.

2. Amplifier Design

Fig. 1 shows the schematic diagrams of the original and modified circuit topologies. For this experiment, the HBT circuit in [2] was implemented using NMOSFETs, as shown in Fig. 1(b). This circuit avoids the use of PMOS transistors, which can provide unwanted capacitance at the output node of the amplifier [1]. As well, the addition of resistor R_2 raises the gain

significantly, as will be shown, without a corresponding decrease in bandwidth. The stage in Fig. 1 may be cascaded with similar stages if source followers are placed between each stage. The loss through these source followers is more than compensated by the added gain provided by resistor R_2 . A complete MA may be designed using an input stage, followed by the circuits in Fig. 1 in the middle stages, and terminated in an output match stage. The input stage is required in order to buffer large input signals (> 1 Volt) and so a special design, such as a cascode differential pair, may be required in this case.

The differential mode half-circuit [3] of the amplifier in Fig. 1(b) is shown in Fig. 2 along with the most significant parasitic elements. The low frequency small signal gain of this circuit is given by

$$\frac{V_{out1}}{V_{in}} = \frac{g_{m1}(R_1 + R_2)(1/g_{m5} + R_f)}{2(1/g_{m3} + R_1)}. \quad (1)$$

This gain is significantly higher than the gain of a MOS Cherry-Hooper amplifier without R_2 or source follower feedback.

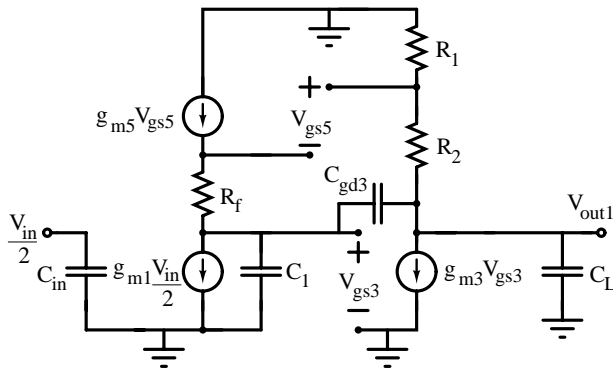


Figure 2. MOS Cherry-Hooper amplifier small signal half circuit.

In the circuit in Fig. 2, the gate-drain capacitance of M_1 , C_{gd1} , was reflected to the gate and drain of M_1 using the Miller effect. Hence, C_1 includes C_{gd1} reflected to the drain of M_1 , the drain-bulk capacitance of M_1 , and the gate-source capacitance of M_3 . Capacitor C_L represents the total capacitance at the output node. The transfer function of this circuit is given by equation (2). The input capacitance C_{in} , when combined with the output resistance of the previous stage, creates a single pole. Capacitors C_1 , C_{gd3} , and C_L combine to create two

$$\frac{V_{out1}}{V_{in}} = \frac{1}{A(1+sR_sC_{in})} \frac{g_{m1}(R_1 + R_2)(1 + g_{m5}R_f)(g_{m3} - sC_{gd3})}{s^2 + \frac{s}{A}\{C_1(R_f g_{m5} + 1) + C_L g_{m5}(R_1 + R_2) + C_{gd3}B\} + \frac{g_{m5}}{A}(1 + g_{m3}R_1)} \quad (2)$$

$$A = (R_1 + R_2)(1 + R_f g_{m5})(C_1 C_L + C_1 C_{gd3} + C_L C_{gd3})$$

$$B = 1 + R_f g_{m5} + R_2 g_{m3} + R_1 g_{m3}(1 + g_{m5}R_f) + R_2 g_{m5}(1 + g_{m3}R_f)$$

additional poles. These two poles will dominate if the pole due to C_{in} and the zero caused by C_{gd3} are at a relatively high frequency. In this case, this circuit is essentially a second-order system. The pole quality factor, Q , may be calculated for the two dominant poles [4]. For $Q > 0.5$, the poles are complex conjugates, a condition required in order to achieve a high gain-bandwidth product. The designer may choose values of Q such as $Q = 1/\sqrt{2}$ corresponding to the maximally flat magnitude response or $Q = 1/\sqrt{3}$ corresponding to the maximally flat delay response. Since the poles are complex, the bandwidth limitations typical of cascaded differential pairs in MAs described in [1] are avoided in this circuit to some extent.

Fig. 3 shows the simulated frequency response of a modified Cherry-Hooper amplifier in a 3.3 V, 0.35 μm CMOS technology along with the response calculated from the model in Fig. 2. The simulation was done using the commercial 0.35 μm CMOS technology file in Spectre but without layout parasitics in order to check the validity of equation (2). Despite its simplicity, the analytic model predicts the frequency response with close accuracy. This allows for accurate initial design of the amplifier without the use of circuit design software.

2. Measurements

In order to measure the amplifier frequency response, a test circuit was fabricated in a 0.35 μm CMOS technology. This is the first published implementation of this circuit in CMOS, to our knowledge. The input and output buffers shown in Fig. 4 were used in order to match the amplifier input and output impedances to 50 Ω . A die photograph of the integrated circuit is shown in Fig. 5. Also included on the chip are the input and output buffers connected directly together in order to measure the loss through these structures.

The fabricated amplifier uses a minimum gate length of 0.5 μm . This length was chosen larger than the process minimum to ensure a small g_{ds} and accurate modelling. Higher bandwidths are achievable with a smaller gate length. The amplifier core consumes 6.0 mA from the 3.3 V power supply.

The measured frequency response of the amplifier test circuit is shown in Fig. 6 along with the simulated response including the effect of parasitic layout capacitances. As shown, the measured and simulated responses are reasonably close. The slightly lower

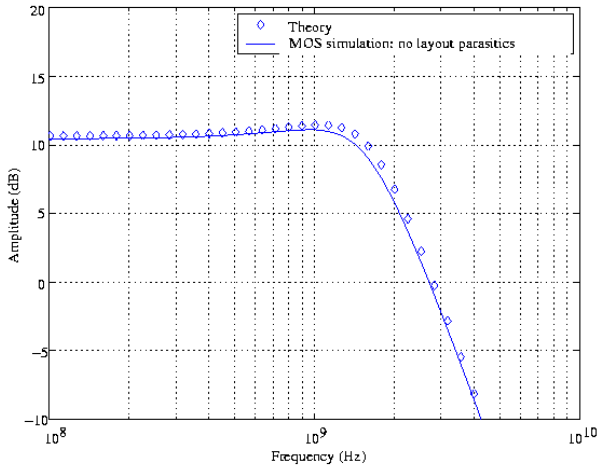


Figure 3. Theoretical and simulated amplifier frequency response.

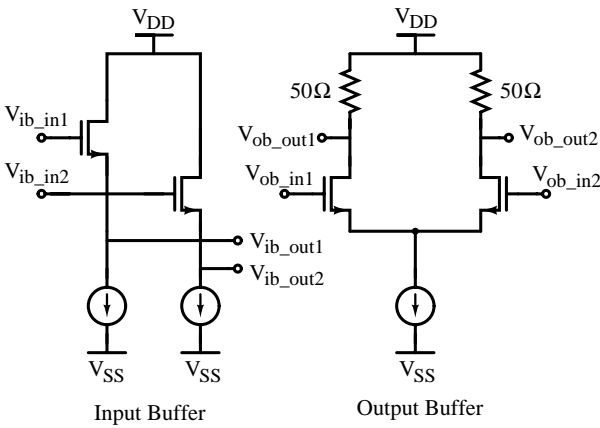


Figure 4. Input and output buffers.

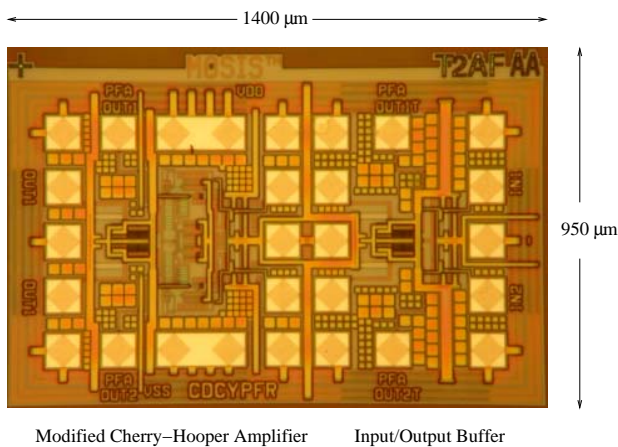


Figure 5. 0.35 μm MOS amplifier test circuit.

measured response is likely due to the inability to simulate parasitic resistances in the design kit. The measured gain and bandwidth are 9.4 dB and 880 MHz, compared to 10.4 dB and 895 MHz for the simulated values.

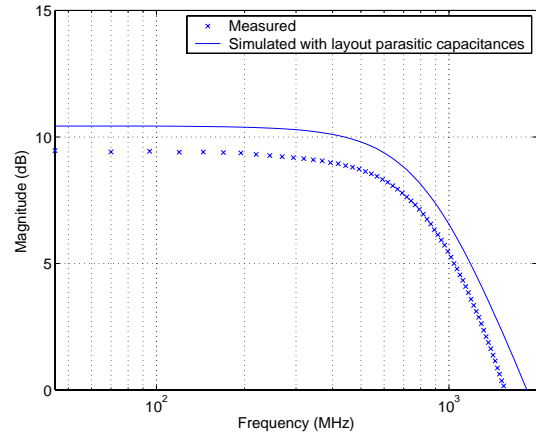


Figure 6. Measured and simulated small-signal amplifier frequency response.

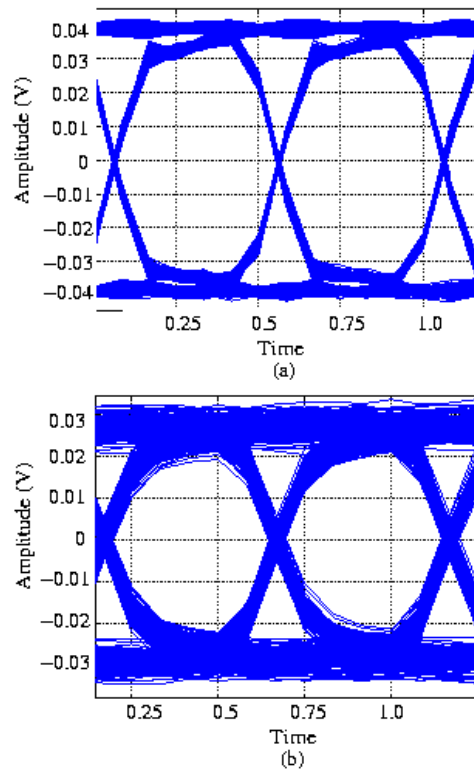


Figure 7. Eye diagrams for 630 MS/s for a) the generator output and b) the amplifier output.

Fig.7 shows the eye diagrams for the pattern generator output and the amplifier output for a 630 MS/s pseudo random bit sequence with a length of $2^{11} - 1$, to test the large signal high speed response. As shown, the amplifier has a good eye opening at this data rate. The measured rise and fall times of the amplifier with the test buffers is approximately 1.25 ns.

A second test circuit that was fabricated and measured is a six stage MA. It has a differential pair input buffer, four of the modified Cherry-Hooper stages in Fig. 1b)

Table 1. Comparison with previous work.

Circuit	Differential Gain	Bandwidth	Noise Figure at 1 GHz	Power Consumption	Supply Voltage
Sackinger and Fischer [4]	32 dB	3 GHz	16 dB	53 mW	3.4 V and 2.5 V
This Work	43 dB	2.1 GHz	14.2 dB	79.2 mW	1.8 V

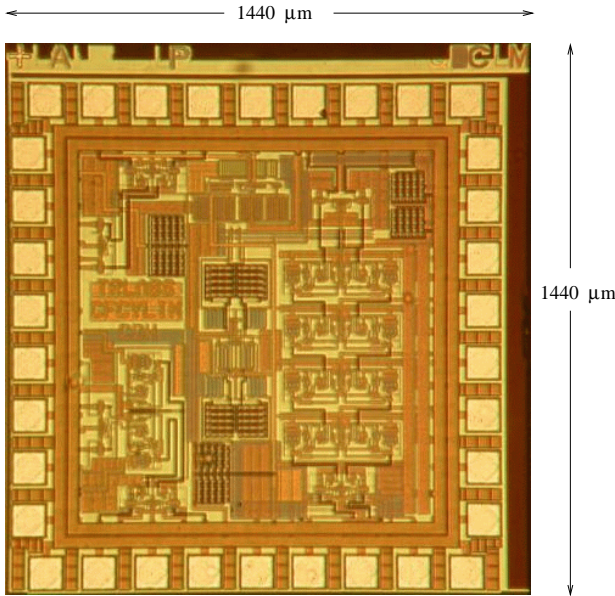


Figure 8. Six stage 0.18 μm CMOS main amplifier.

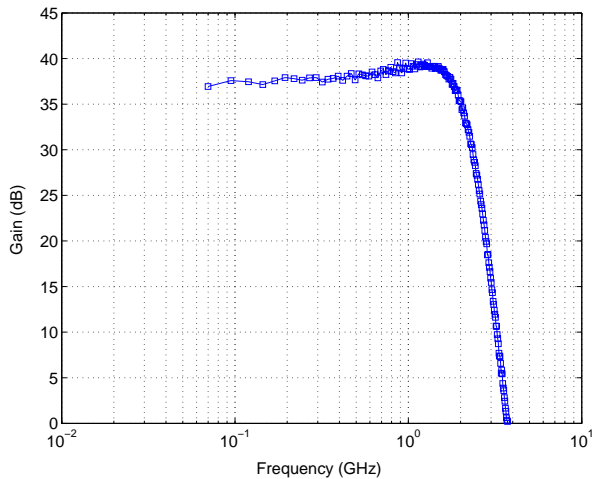


Figure 9. Magnitude response of six stage MA.

cascaded with source followers used in between each stage, and a differential pair output buffer. It consumes 44 mA from a single 1.8 Volt supply (79.2 mW) and was fabricated in 0.18 μm technology. A chip photograph is shown in Fig. 8. The active area of the circuit is 0.77 mm^2 .

The measured single ended gain of the differential MA versus frequency is shown in Fig. 9. The single ended gain is 37 dB and the bandwidth is 2.1 GHz. The

measured noise figure of the amplifier is 14.2 dB at 1GHz. The slight gain peaking is undesirable and may be avoided in future implementations by choosing a lower Q for the Cherry-Hooper stage poles.

This MA is compared with a previous work [4] in Table 1. The MA presented here has significantly more gain, a lower noise figure, and avoids the extra supply voltage needed by active inductors.

2. Conclusions

A modification to the standard MOS Cherry-Hooper amplifier was presented. It was shown that this stage may be modelled as a second order system based on a pair of complex conjugate poles. Furthermore, the modified circuit has a significantly higher gain than the standard Cherry-Hooper amplifier.

A test circuit of the modified Cherry-Hooper stage was implemented in a 0.35 μm CMOS technology. The measurements showed a gain of 9.4 dB and 880 MHz bandwidth. As well, the measured and simulated frequency responses matched with close accuracy.

A high performance MA that uses these stages was presented. It has a low noise figure of 14.2 dB, and uses only one supply voltage.

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