A Limiting Amplifier using Modified Cherry-Hooper Stages in 0.18 µm CMOS

UNIVERSITY OF CALGARY

ATIPS

Research Objectives

- To improve previously published limiting amplifiers by eliminating the extra supply voltage or chip area needed by inductively peaked gain stages.
- To verify an amplifier modeling procedure developed by the authors.

Cherry-Hooper Stage Design

Fig. 1 shows a Cherry-Hooper amplifier with source follower feedback. It is an implementation of a design used previously only with bipolar transistors.

Modeling techniques for this circuit unique to CMOS were developed. Fig. 2 shows the most important elements in the amplifier.

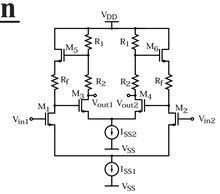


Figure 1 - Modified Cherry-Hooper stage.

The transfer function of the amplifier is given in equation (1).

$$\frac{V_{out1}}{V_{in}} = \frac{1}{A(1+sR_LC_{in})} \frac{g_{m1}(R_1+R_2)(1+g_{m5}R_f)(g_{m3}-sC_{gd3})}{s^2+\frac{s}{A}\left\{C_1(R_fg_{m5}+1)+C_Lg_{m5}(R_1+R_2)+C_{gd3}B\right\}+\frac{g_{m5}}{A}(1+g_{m3}R_1)} \quad (1)$$

$$A=(R_1+R_2)(1+R_fg_{m5})(C_1C_L+C_1C_{gd3}+C_LC_{gd3})$$

$$B=1+R_fg_{m5}+R_2g_{m3}+R_1g_{m3}(1+g_{m5}R_f)+R_2g_{m5}(1+g_{m3}R_f)$$

From the equation, the system is seen to be second order with a transfer function of the form

$$\frac{V_{out1}}{V_{in}} = \frac{1}{s^2+s\frac{\omega_o}{Q}+\omega_o^2}$$

The pole quaulity factor Q determines the response.

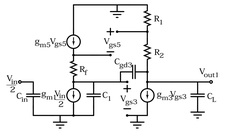


Figure 2 - Small signal half circuit.

Fig. 3 compares the simulated response and the response from equation (1).

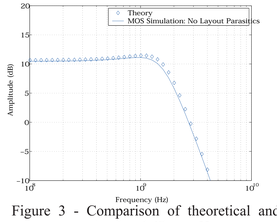


Figure 3 - Comparison of theoretical and simulated Cherry-Hooper stage response.

Application: Optical Receivers

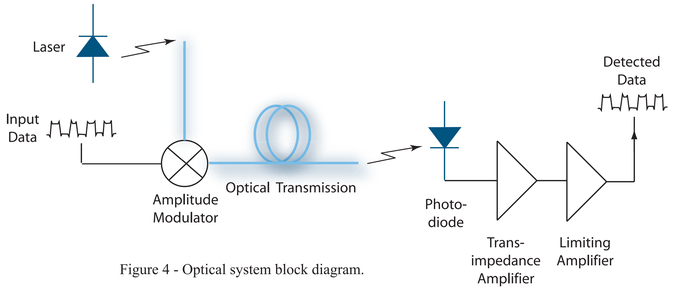


Figure 4 - Optical system block diagram.

Limiting Amplifier Circuit

Modified Cherry-Hooper Stage with Source-Follower Feedback and Source Follower Output Buffers

Input Buffer and Match

Output Buffer and Match

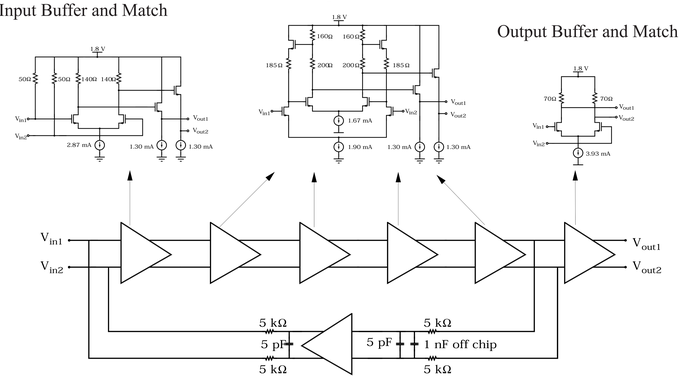


Figure 6 - Six stage limiting amplifier block diagram.

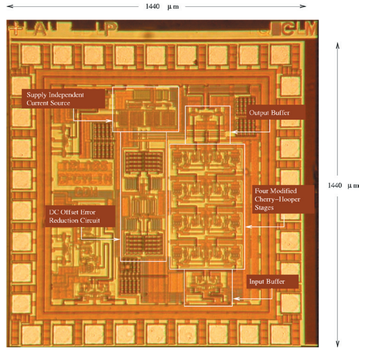


Figure 5 - Chip photograph of limiting amplifier.

Limiting Amplifier Measurements

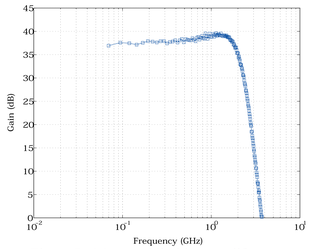
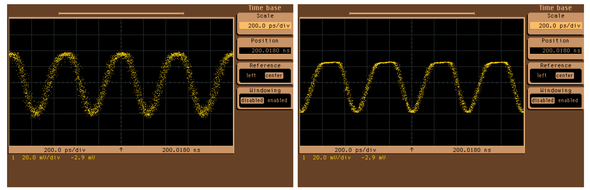


Figure 7 - Measured limiting amplifier response.

The limiting amplifier has a measured single ended gain of 37 dB and a bandwidth of 2.1 GHz.



a) - 50 dBm input

+5 dBm input

Figure 8 - Limiting amplifier large signal response.

Fig. 8 shows the amplifier responses to -50 dBm and +5 dBm input signals. In both cases the amplifier achieves a full 80 mVpp output voltage.

Circuit	Differential Gain	Bandwidth	Noise Figure at 1 GHZ	Power Consumption	Supply Voltage
Sackinger and Fischer	32 dB	3 GHz	16 dB	53 mW	3.4 V and 2.5 V
This Work	43 dB	2.1 GHz	14.2 dB	79.2 mW	1.8 V

Table 1 - Comparison with previous work

This limiting amplifier is compared with a previous work in Table 1. The previous work is based on an active inductor amplifier. The limiting amplifier presented here has significantly more gain, a lower noise figure, and avoids the extra supply voltage needed by active inductors.

Conclusions

In this poster, modified Cherry-Hooper stages using NMOSFETs were introduced. It was shown that these stages may be modeled as a second order system.

A high performance limting amplifier that uses these stages was presented. It has a low noise figure of 14.2 dB, and uses only one supply voltage.

Acknowledgements

This project is funded by:

- The Canadian Microelectronics Corporation
- The Natural Sciences and Engineering Research Council of Canada
- The Alberta Informatics Circle of Research Excellence

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Chris D. Holdenried and James W. Haslett - University of Calgary ATIPS Laboratory

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