

What is the GigaRFIC project?

Giga - Researchers at TR Labs have developed a prototype 4th generation wireless LAN capable of data rates in excess of 1 gigabit per second. It is called the **Gigabit Radio**.

RFIC - **R**adio **F**requency **I**ntegrated **C**ircuit. A single radio component or an entire radio transceiver integrated onto a single chip.

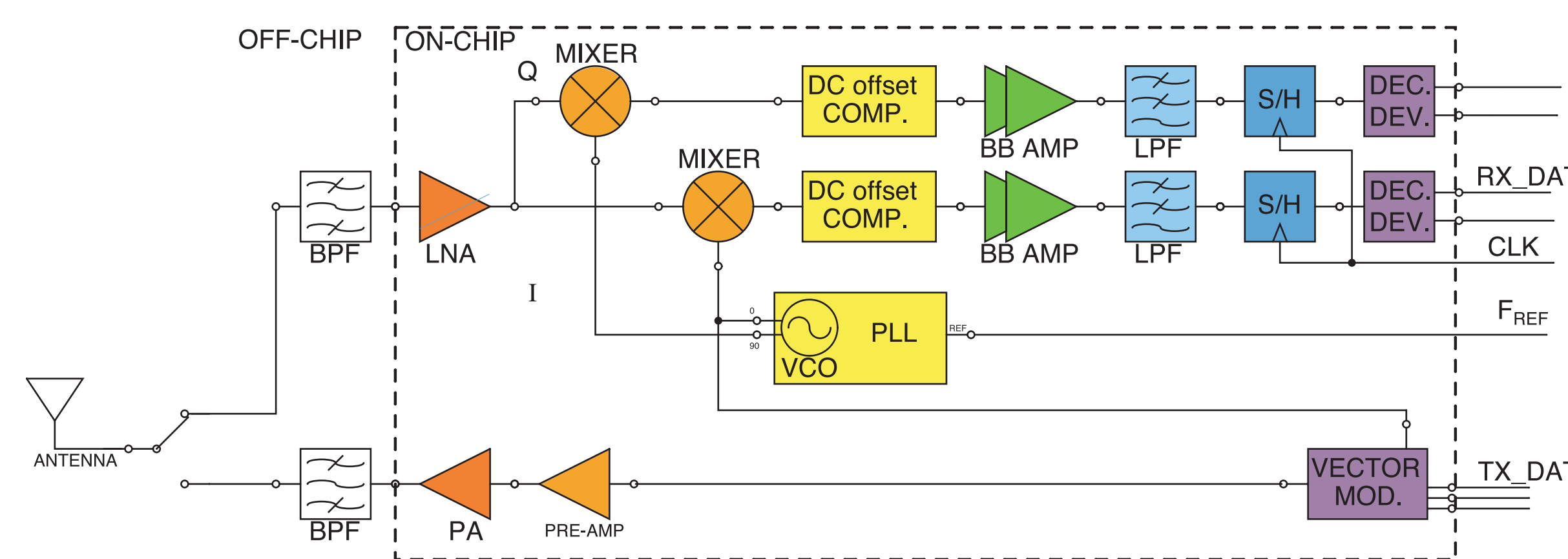
The **GigaRFIC** project is aimed at creating RFIC components for the terminal devices of the TR Labs Gigabit Radio. The long-term goal is a single "Gigabit Radio-on-a-Chip".

Design Considerations

With the radical nature of the Gigabit Radio come some interesting design challenges and opportunities for the GigaRFIC components:

- **High GHz Operation** - A large piece of continuous RF spectrum is required for gigabit-per-second transmission. The Gigabit Radio system uses 400 MHz of bandwidth centered at 17.35 GHz. This frequency band is considerably higher than the 2.4 GHz and 5 GHz bands of conventional wireless LANs.
- **Wide Channel Bandwidth** - The baseband circuitry must handle signals with 200 MHz of bandwidth; much higher than conventional wireless LANs.
- **Low Bit Error Rate (BER)** - Another system goal is to achieve very low BERs. However the wide bandwidth of the channel raises the input noise floor. RFIC blocks must be designed with a minimized noise figure to compensate.
- **Simplicity** - The terminal should be highly integrated, simple, and should not consume excessive amounts of power.

The GigaRFIC Transceiver



The GigaRFIC transceiver block diagram is shown in the above figure. The receiver uses direct conversion which offers the following benefits:

- **Reduced number of off-chip components**
- **Higher degree of integration**
- **Reduced number of RFIC blocks**
- **Multi-band/Multi-standard capabilities**

However, direct conversion receivers also have several design challenges:

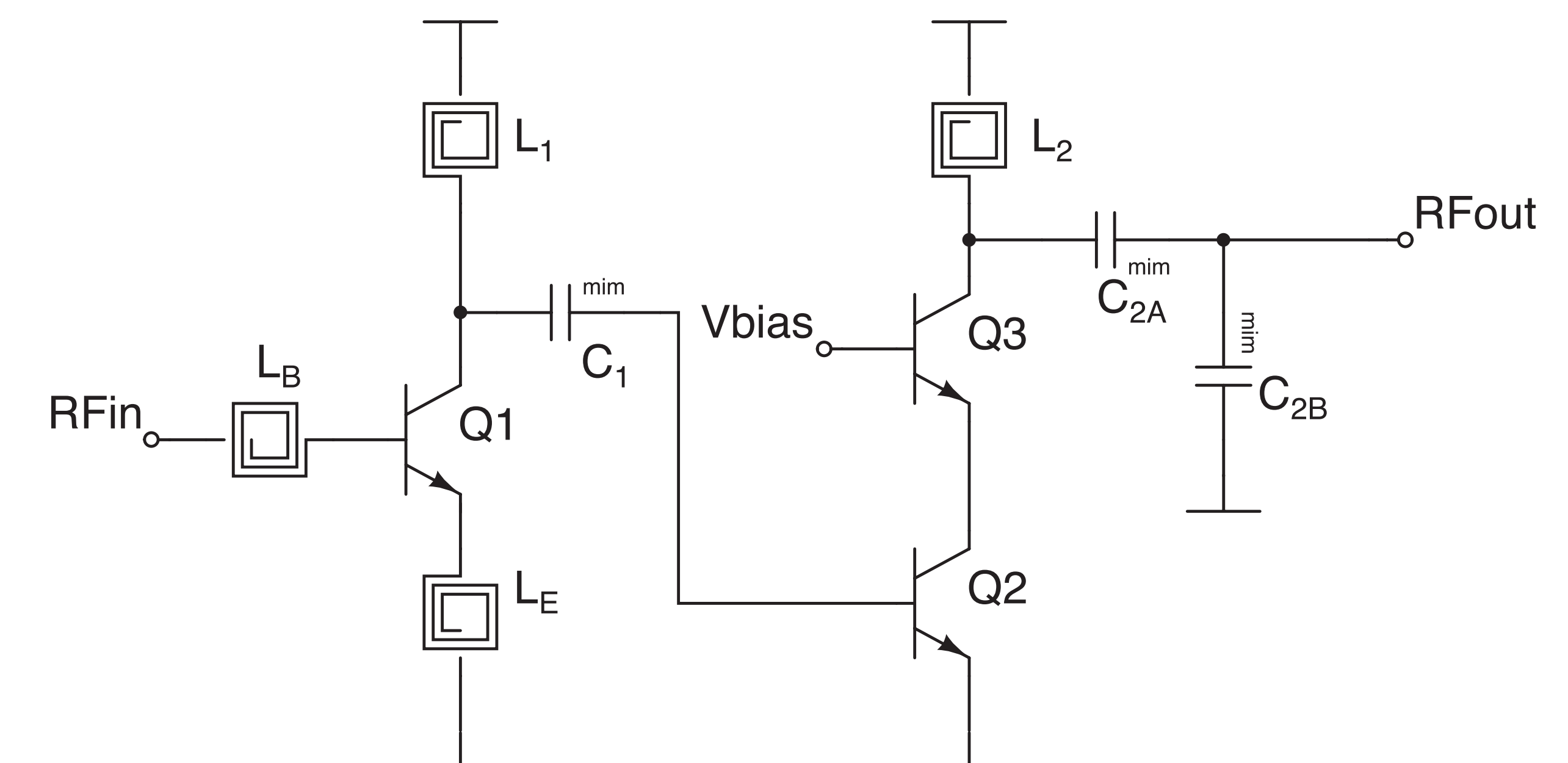
- **DC offsets**
- **I/Q phase and amplitude mismatch**
- **Even-Order Distortion**
- **Flicker Noise**

Fortunately, there exist several circuit and system solutions to the above problems.

The GigaRFIC transceiver also features a simple transmit-path. The local oscillator tone is modulated directly with digital bits from the baseband section. A vector modulator adjusts the LO signal phase accordingly. This eliminates the need for a high speed D/A converter.

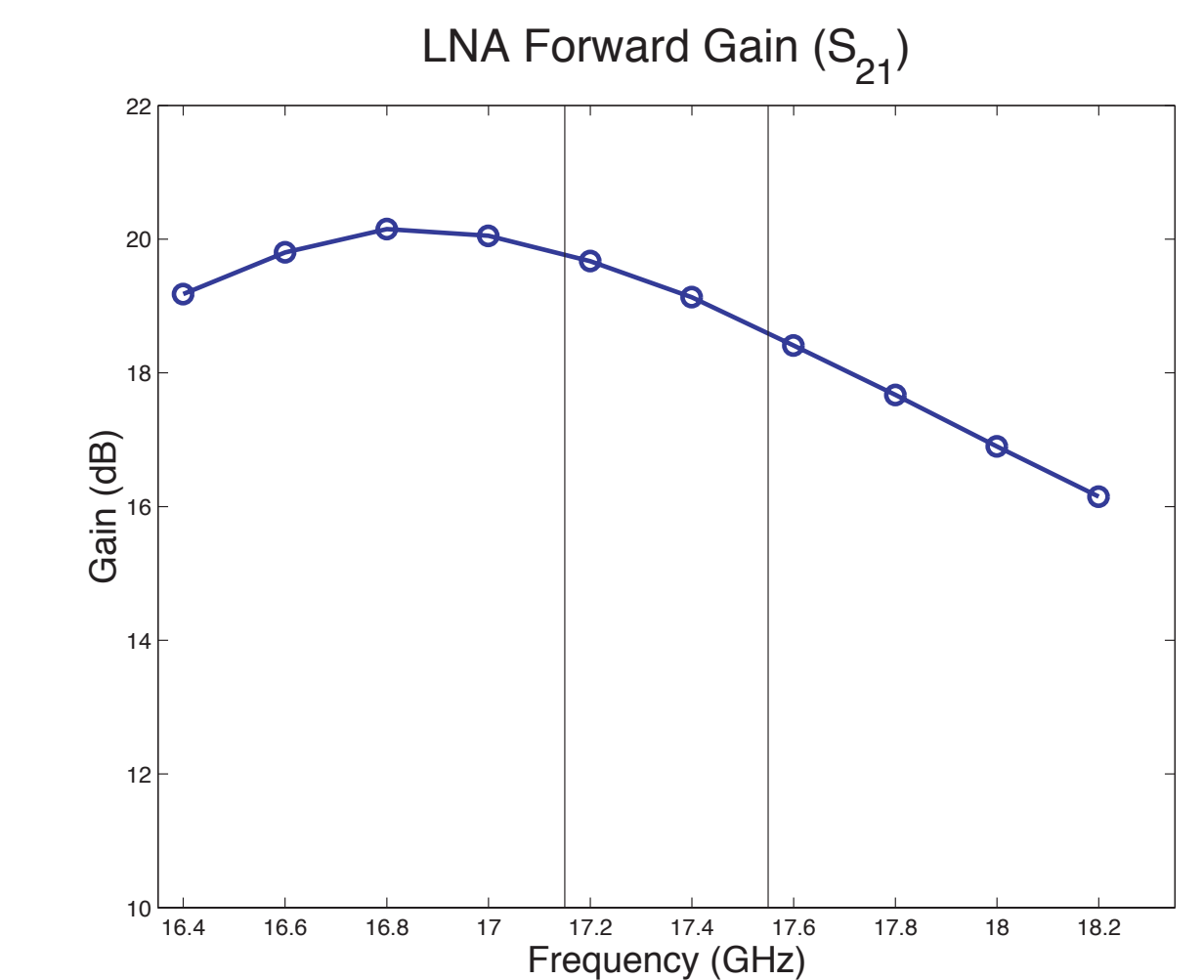
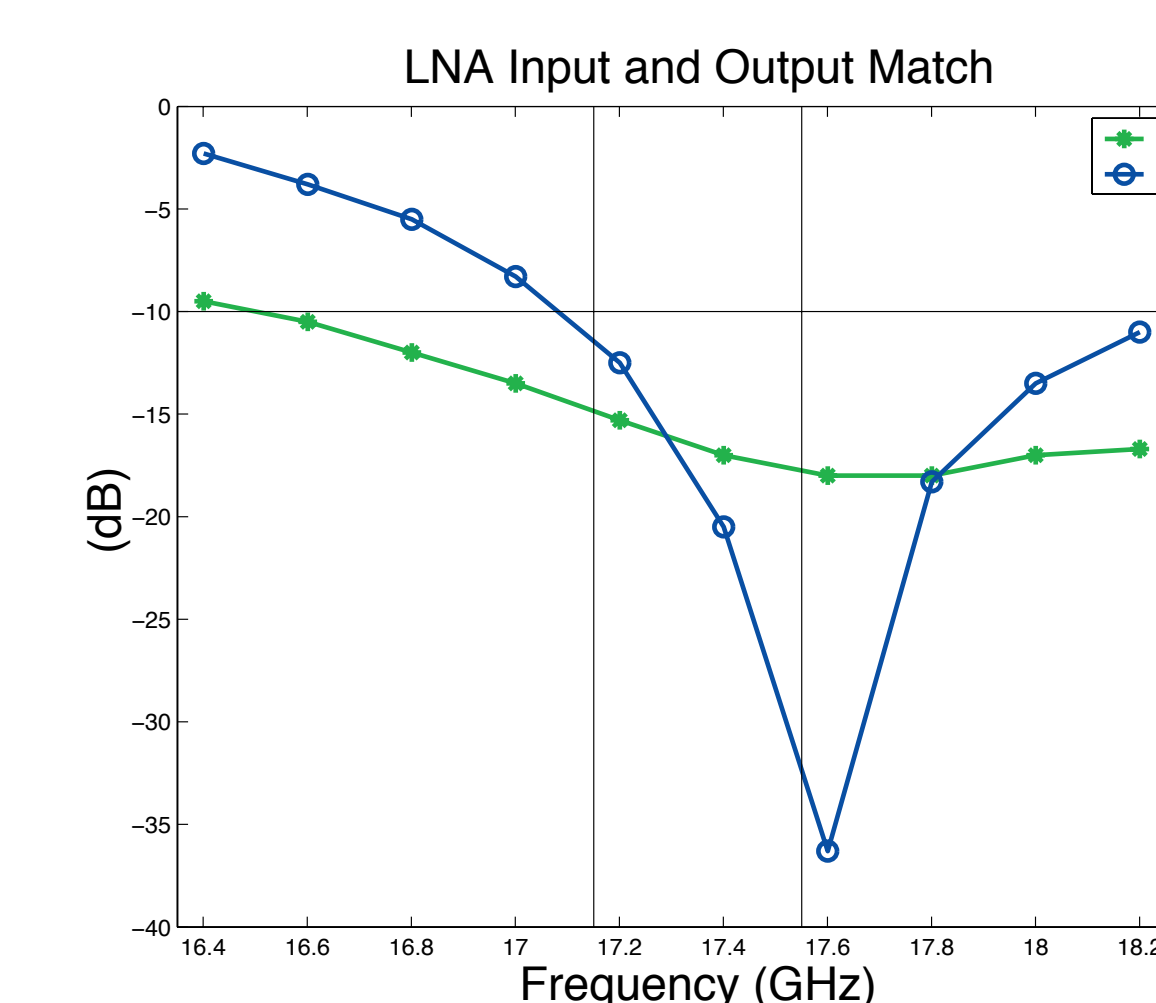
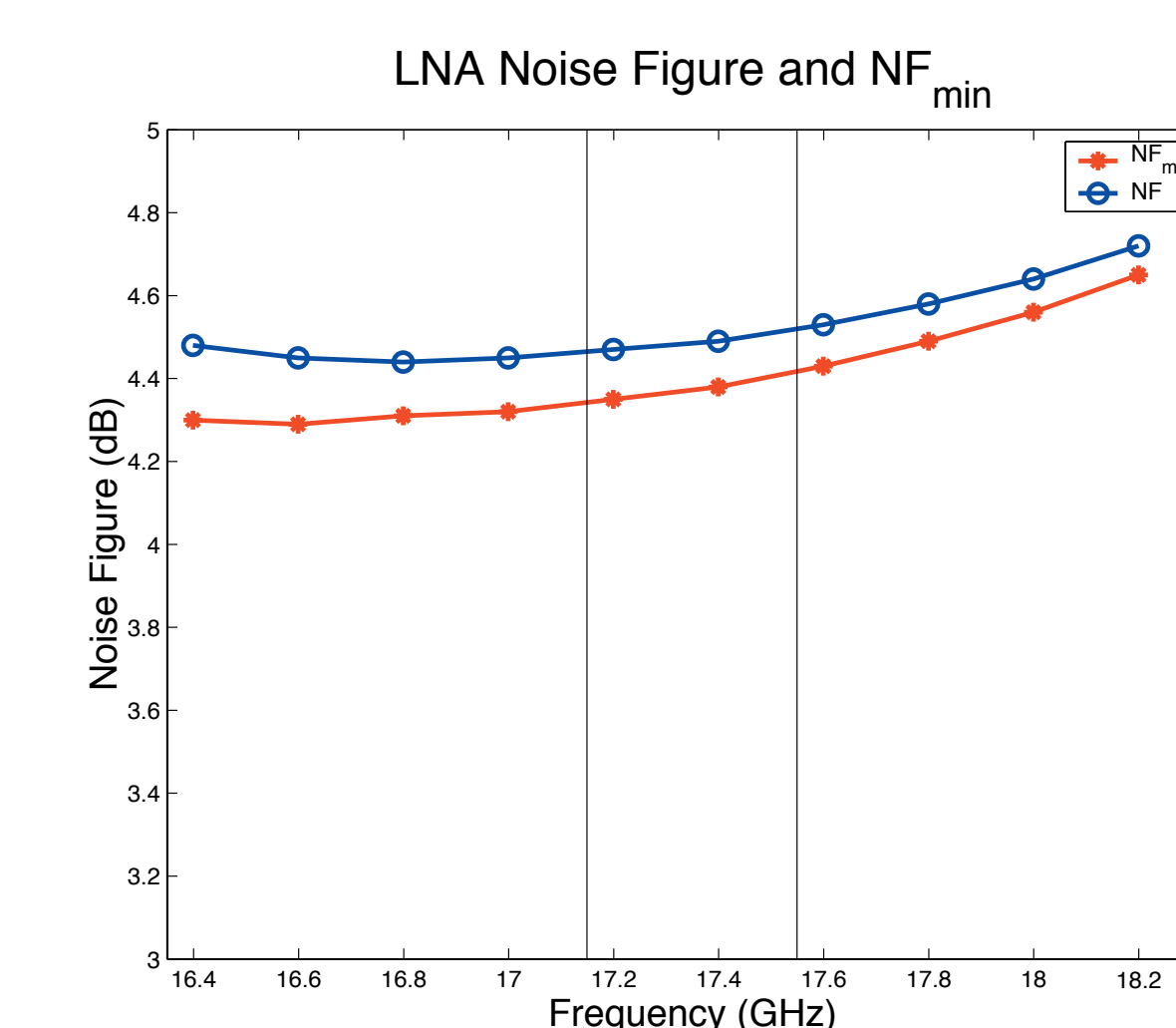
This poster will present the first results for the GigaRFIC receiver: a low noise amplifier (LNA) and a mixer.

17 GHz Low Noise Amplifier

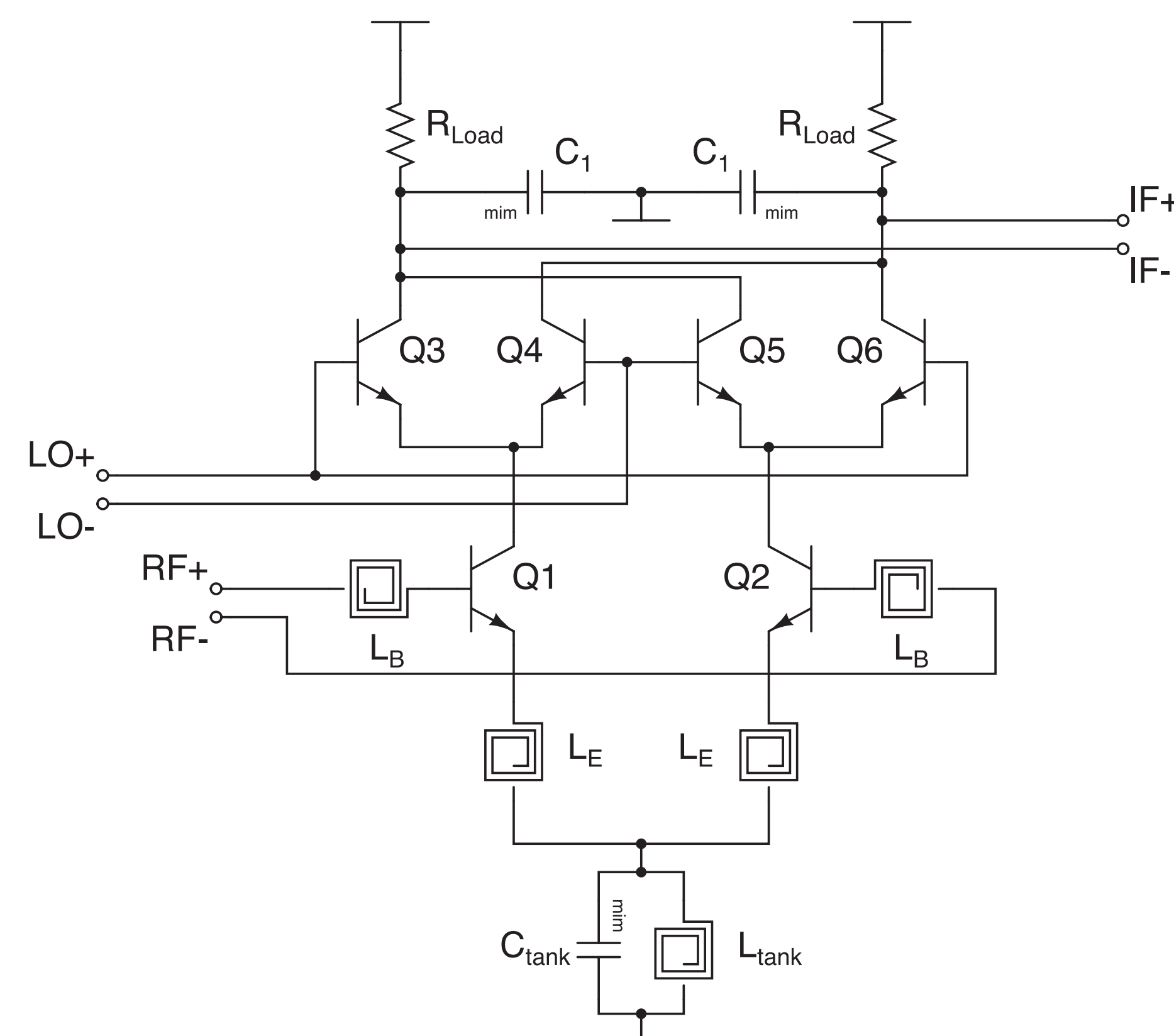


The schematic for the 17.35 GHz low noise amplifier (LNA) is shown in the above figure. It is a two-stage design. The first stage uses a single common-emitter transistor with inductive degeneration. This stage is noise and power matched to 50 Ω. The second stage uses two transistors in cascode. This stage is optimized to increase LNA gain.

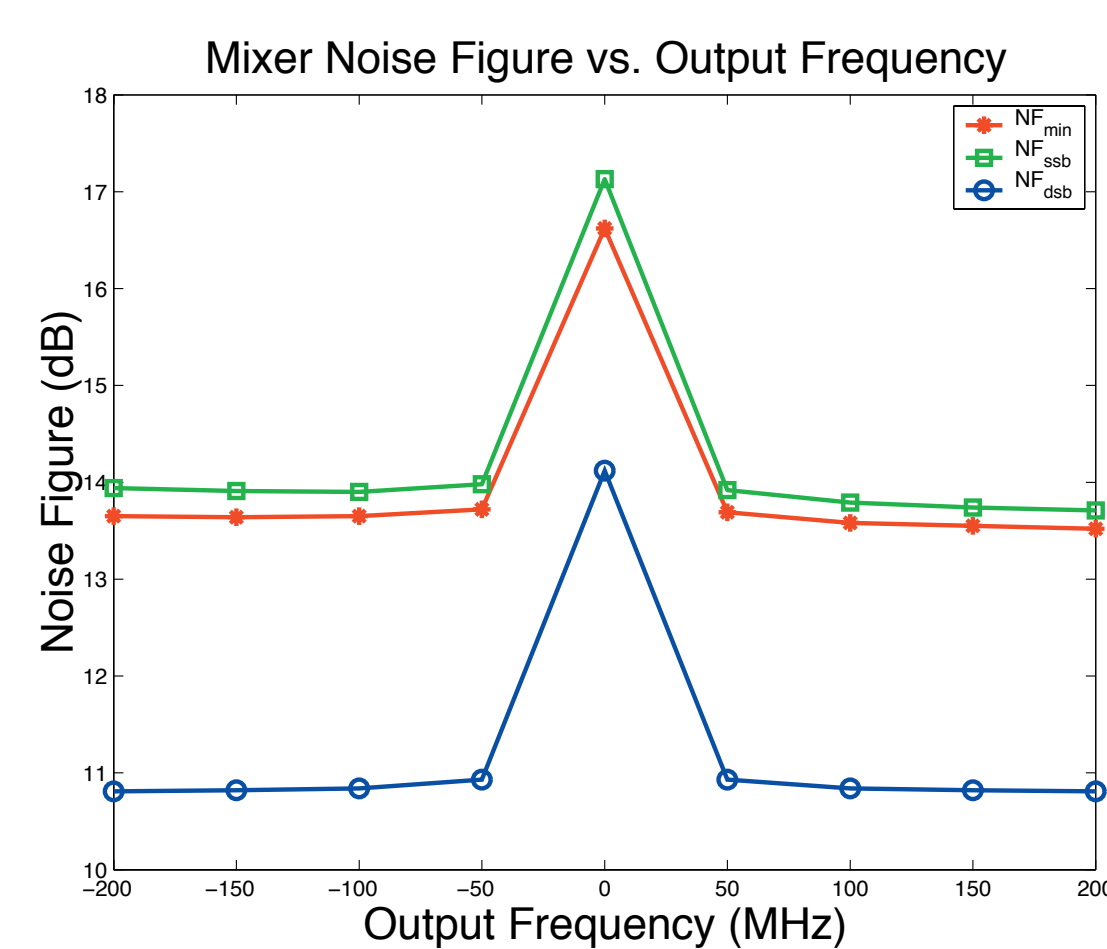
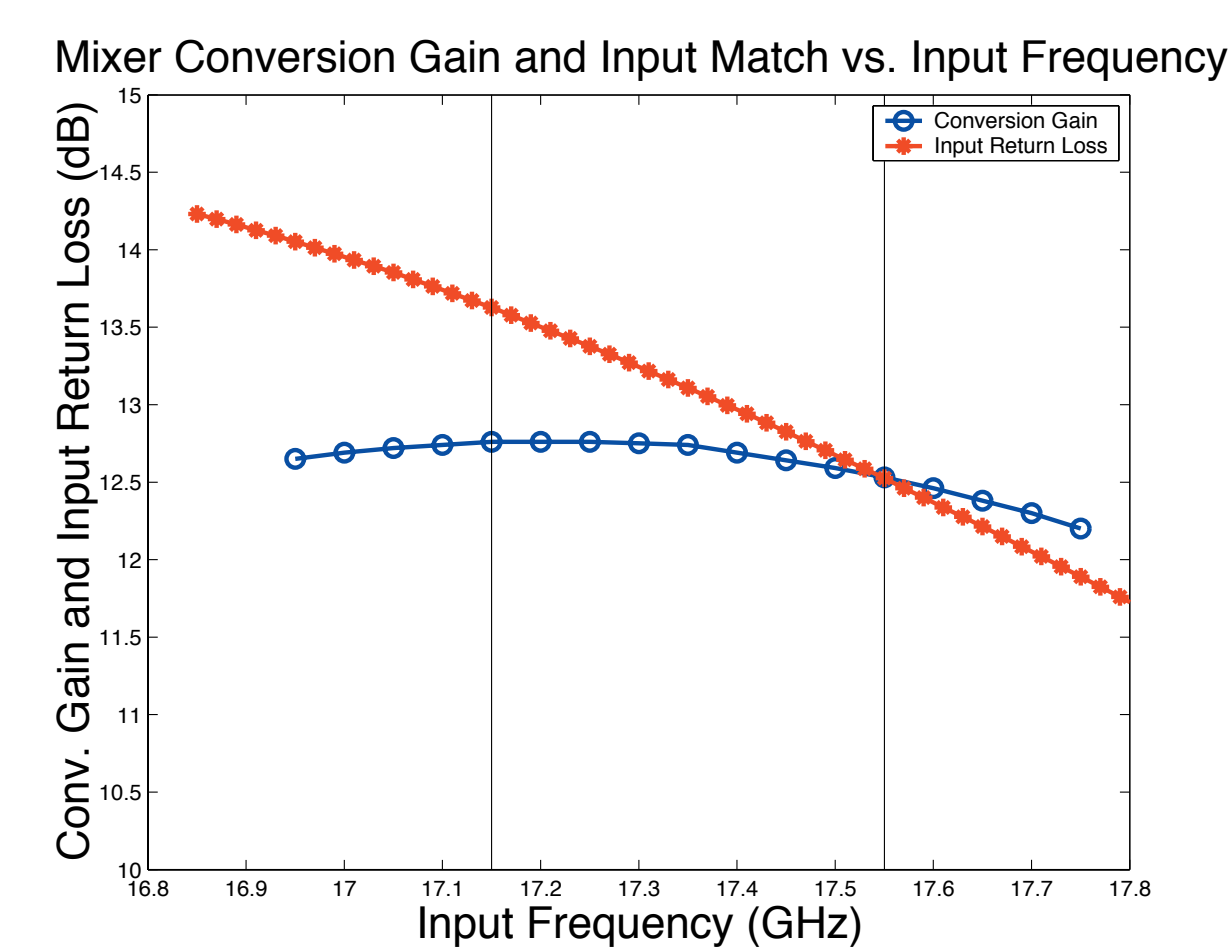
These plots show simulated LNA performance (with layout parasitics). The LNA achieves 19.2 dB gain and 4.5 dB noise figure. S₁₁ is below -10 dB and the noise figure is very close to NF_{min}. The LNA is simultaneously noise and power matched to 50 Ω.



17 GHz Mixer



The schematic for the 17.35 GHz mixer is shown in the above figure. The fully balanced mixer uses the same noise and power matching techniques used in the LNA. To maximize headroom, the tail current source is replaced with a resonant tank. The mixing quad transistors Q3-Q6 are sized smaller to maximize f_T . This reduces noise that results from imperfect switching.



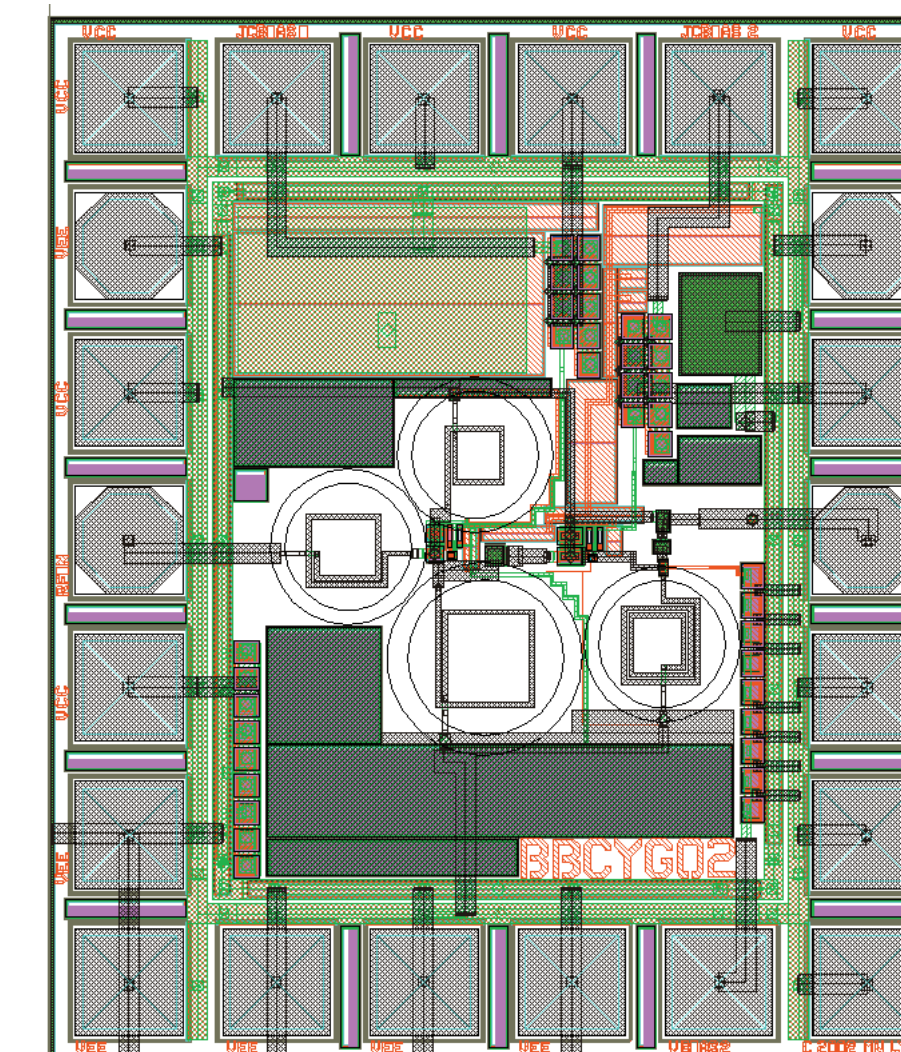
The simulated mixer performance (with extracted layout parasitics) is shown in the above figures. The conversion gain is 12.7 dB. The double sideband noise figure is 10.8 dB. The mixer is simultaneously noise and power matched to 50Ω. This can be seen from the high input return loss, and the close proximity of the NF_{SSB} and NF_{min} curves.

Implementation

The LNA and mixer were implemented in IBM's 5HP process. It is a SiGe BiCMOS process that features bipolar transistors with enhanced RF performance. (peak $f_T=47$ GHz). The process has a $2\mu\text{m}$ thick third level metal for implementing inductors as well as $0.7\text{ fF}/\mu\text{m}^2$ MiM capacitors.

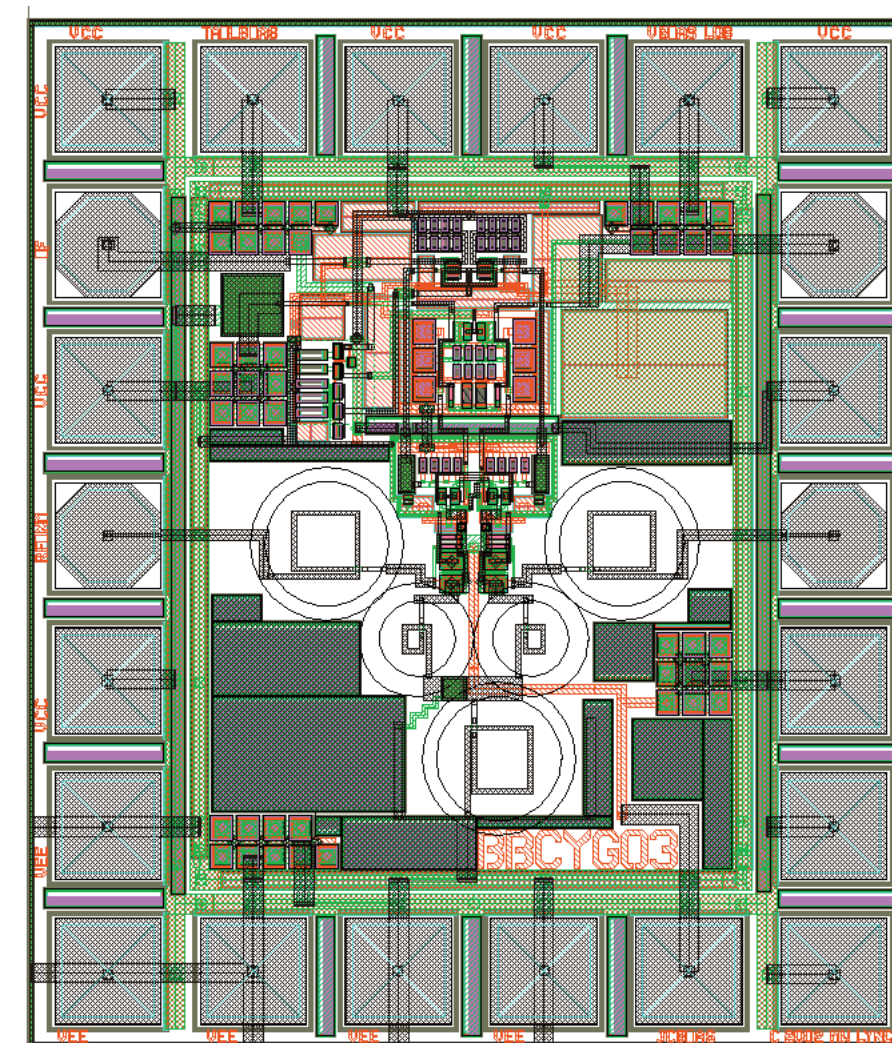
IBBCYG02 - 17 GHz LNA

- Uses on-chip spiral inductors
 - (200 pH - 700 pH)
- On chip decoupling capacitors
- Parasitics minimized through careful layout



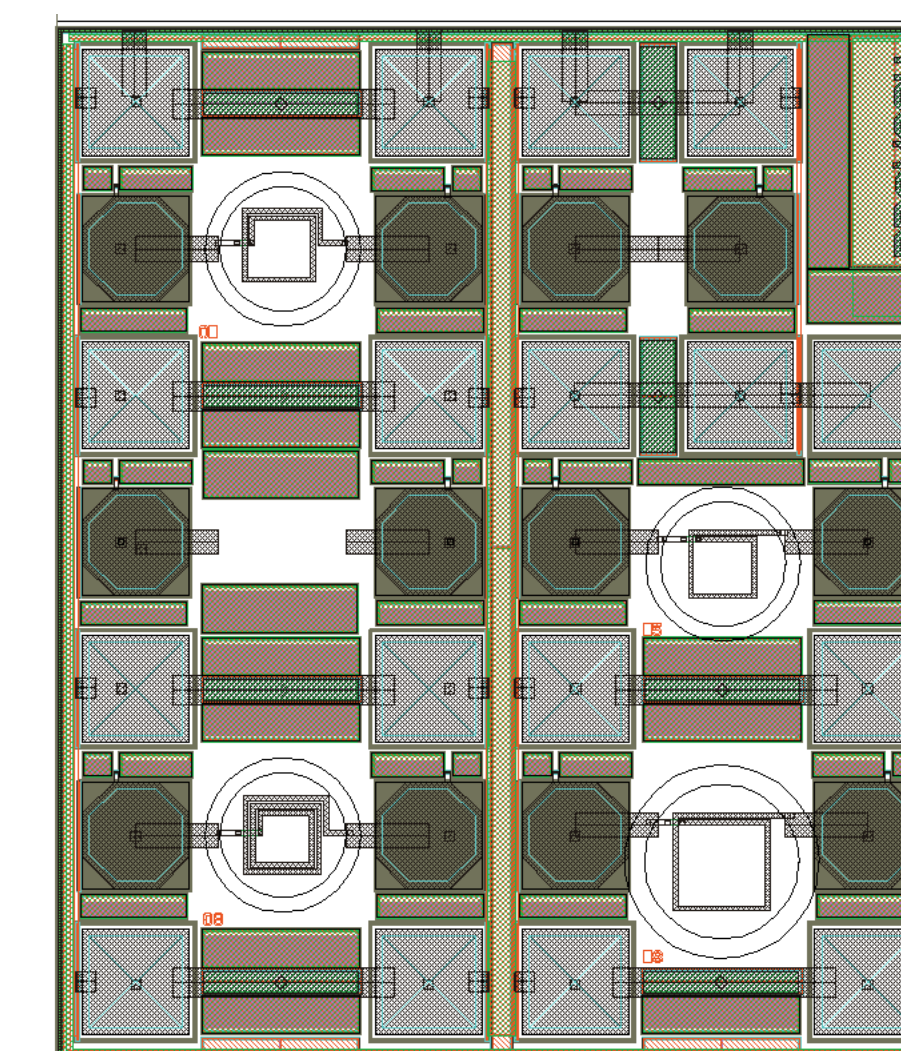
IBBCYG03 - 17 GHz MIXER

- Includes LO buffer and baseband amplifier for ease of test
- Uses on-chip spiral inductors
 - (70 pH - 300 pH)
- On chip decoupling capacitors
- Parasitics minimized through careful layout and symmetry



IBBCYG04 - picoHenry Inductors

- For characterization of spiral inductor models.
- Inductors designed with ASITIC, Ansoft HFSS and Cadence Spiral Inductor Modeler.

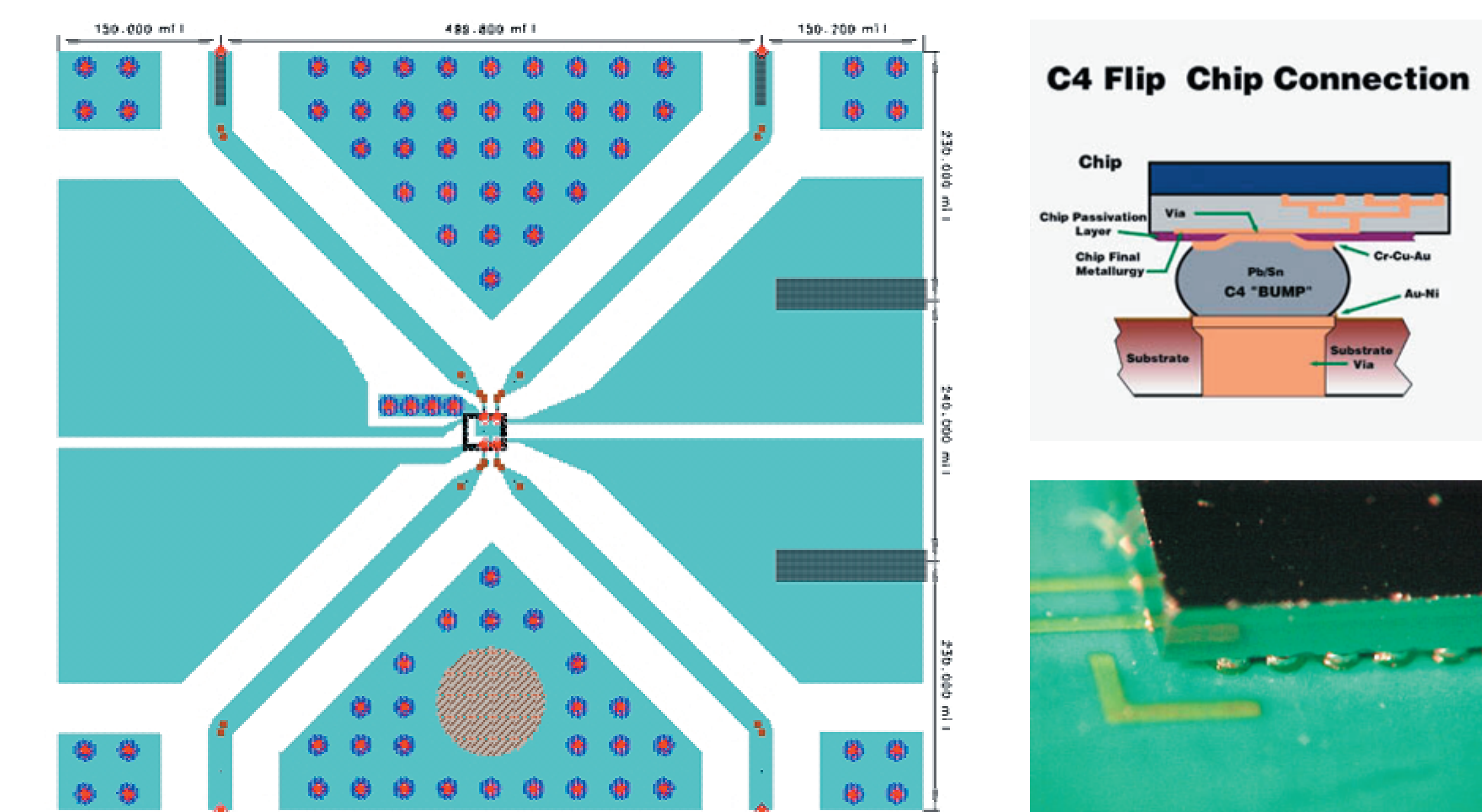


Testing

Bare die will be mounted on test substrates. DC bias will be supplied through bond wires. The devices will be tested with two G-S-G-S-G wafer probes.

Additionally, chips will be flip-chip mounted onto a carrier with microstrip traces. These carriers will then be placed in a shielded test jig for testing. Flip-chip services are being piloted through CMC.

A depiction of flip-chip mounting and the microstrip test carrier are shown below.



Summary

The GigaRFIC project is an on-going research endeavor at the University of Calgary and TRILabs. 17GHz RFIC components are being developed for transceiver-on-a-chip applications. This poster presents first results for a 17 GHz LNA and mixer.

Acknowledgements

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