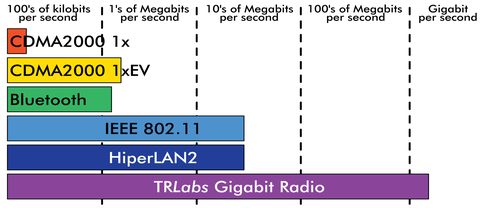
A Novel Gigabit Radio Transceiver for System-on-a-Chip Wireless LAN

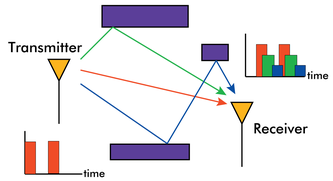
ATIPS

Wireless Data Rates

Conventional wireless data rates are limited to 10's of megabits per second. This is much less than the data rates for wired or optical networks. The figure below presents an overview of current and future wireless data rates. The reduced wireless data rates create bottlenecks for high data rate applications such as high quality video.



High data rate transmission is made difficult by the effects of multipath within the wireless channel. Multiple versions of the transmitted signal arrive at different times due to different path lengths. As symbol rates increase, inter-symbol interference occurs.



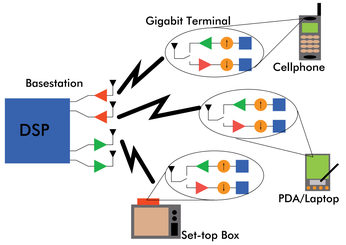
The Gigabit Radio

Researchers at TRLabs are developing networks for the future that address these problems. The Gigabit Radio is one such network. Powerful DSP techniques are used at the basestation to compensate for multipath in the channel. Data rates in excess of 1 gigabit per second are possible. With powerful DSP in the basestation, the terminals can be simple devices with minimal signal processing.

What is the GigaRFIC project?

An RFIC is a Radio Frequency Integrated Circuit. It can be a single radio component, or an entire radio system integrated on a chip.

The GigaRFIC project is aimed at creating RFIC components for the terminal devices of the TRLabs Gigabit Radio. The long-term goal is a single "Gigabit-Radio-on-a-Chip". These terminal chips can then be incorporated into electronic devices such as cellphones, laptops, or TV set-top boxes.



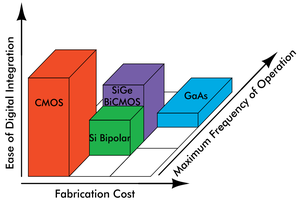
Design Considerations

With the radical nature of the Gigabit Radio come some interesting design challenges and opportunities for the GigaRFIC components:

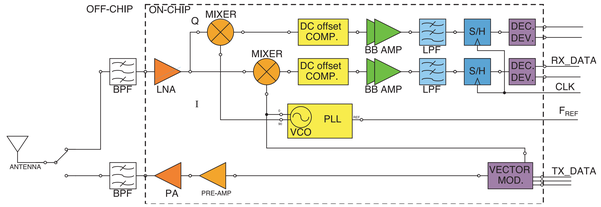
- **High GHz Operation** - A large piece of continuous RF spectrum is required for gigabit-per-second transmission. The Gigabit Radio system uses 400 MHz of bandwidth centered at 17.35 GHz. This frequency band is considerably higher than the 2.4 GHz and 5 GHz bands of conventional wireless LANs.
- **Wide Channel Bandwidth** - The baseband circuitry must handle signals with 200 MHz of bandwidth; much higher than conventional wireless LANs.
- **Low Bit Error Rate (BER)** - Another system goal is to achieve very low BERs. However the wide bandwidth of the channel raises the input noise floor. RFIC blocks must be designed with a minimized noise figure to compensate.
- **Simplicity** - The terminal should be highly integrated, simple, and should not consume excessive amounts of power.

Process Selection

Several fabrication options exist for RFICs. These range from high performance, but expensive GaAs, to low cost and lower performance CMOS. However to achieve the performance required at 17GHz, and to allow digital CMOS integration, a SiGe BiCMOS process has been selected for fabrication.



The GigaRFIC Transceiver



Receiver

The GigaRFIC transceiver block diagram is shown in the above figure. The receiver uses direct conversion which offers the following benefits:

- Reduced number of off-chip components
- Higher degree of integration
- Reduced number of RFIC blocks
- Multi-band/Multi-standard capabilities

However, direct conversion receivers also have several design challenges:

- DC offsets
- I/Q phase and amplitude mismatch
- Even-Order Distortion
- Flicker Noise

Fortunately, there exist several circuit and system solutions to the above problems.

Transmitter

Simplicity is again the goal for the transmit path architecture of the GigaRFIC transceiver.

The modulation scheme for up-link to the basestation is phase-shift-keying. Rhe RF carrier's phase is modulated in accordance with the digital bits to be encoded. This constant-envelope modulation scheme allows a highly efficient, non-linear power amplifier to be used inside the terminal.

To accomplish the phase modulation, a vector modulator block is used. It modulates the phase of the RF carrier from the VCO based upon the digital levels of the transmitted bits. This block removes the need for a high speed digital-to-analog converter.

Current Research

Current research is focussed on developing individual RFIC components for the Gigabit Radio Terminal. A low-noise-amplifier (LNA) and mixer have recently been submitted for fabrication. Work has also begun on the design of a voltage-controlled oscillator (VCO), phase lock loop (PLL) and power amplifier. These efforts seek to better understand what circuit capabilities are currently possible at 17GHz.

Summary

The GigaRFIC project seeks to develop RFIC blocks for a gigabit per second wireless LAN. These RFIC blocks can be later implemented as IP cores for further SoC integration.

Acknowledgements

This research is supported by TRLabs, NSERC and iCORE. The Canadian Microelectronics Corporation is acknowledged for their technical support and fabrication services.

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