

©2002 TRILabs. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from TRILabs.

Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

A Novel Gigabit Radio Transceiver for System-on-a-Chip Wireless LAN

The GigaRFIC Project

M.W. Lynch¹, J.W. Haslett¹, G. M^cGibney², A.Garg¹

¹University of Calgary, ² TRILabs

Abstract: This paper presents a plan for creating radio frequency integrated circuit (RFIC) transceiver components for a gigabit per second wireless LAN terminal. The transceiver will operate in the 17-GHz frequency band and be fabricated in a SiGe BiCMOS process. The transceiver will use a direct conversion receiver and a vector modulator for transmission. This paper includes a discussion on direct conversion design issues. The transceiver IC represents a complete RF system. The RFIC blocks can also be incorporated with other IP blocks such as protocol cores for further SoC applications

Key words: wireless, WLAN, RFIC, gigabit-per-second, SiGe, direct-conversion, transceiver, 17-GHz.

1. INTRODUCTION

Conventional wireless data networks such as Bluetooth or IEEE 802.11 offer data rates that are limited to 10⁷s of megabits per second [1],[2]. These data rates are much lower than those for the fibre-optic networks which make up the backbone of networks like the Internet. Thus, there is a “last-mile problem” where the access points to the network, the wireless terminals in this case, become bottlenecks for high data rate applications.

This is compounded by the effects of multipath in the wireless channel which makes high data rate transmission difficult. A brief explanation of these effects is given here with the help of Figure 1. In addition to the direct radio path between transmitter and receiver, there exist many paths that contain one or more reflections. Each path has a different path length which results in multiple versions of the transmitted symbol arriving at the receiver at different instants in time. As symbol rates increase, the time between transmitted signals decreases. If the time between first and last transmission path exceeds the time between transmitted symbols intersymbol interference (ISI) occurs and the data becomes corrupted [3]. The exact point at which ISI occurs depends upon the radio environment, but is inevitable when using high data rate wireless devices.

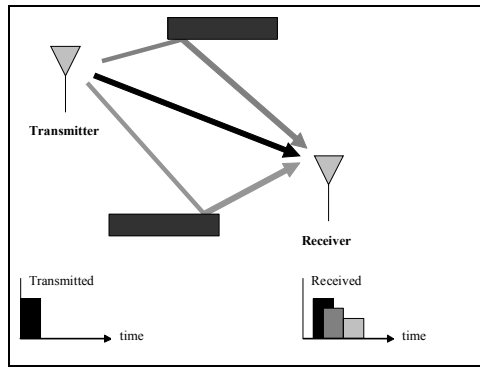


Figure 1. Illustration of multipath in a wireless channel

Researchers at TRILabs are building networks for the future that address these and other problems. The Gigabit Radio project is one such network. Its goal is to transmit data at up to gigabit per second data rates through a wireless channel. Powerful DSP techniques are used to counteract the effects of multipath. However, DSP is costly in terms of complexity, power consumption, and component cost. So the Gigabit Radio places the DSP solely in the basestation, spreading the costs of the DSP across the entire network. The DSP is now used in an asymmetric equalization scheme where data is pre-distorted on the downlink and post-equalized on the uplink back to the basestation. The terminals are left as simple devices with no complex signal processing [4].

Developing the simple terminals in integrated circuit form is the goal of the GigaRFIC project, which is the topic of this paper. The IP-cores for both the radio frequency integrated circuit (RFIC) front-end and baseband protocol back-end could then be incorporated into system-on-a-chip (SoC) solutions for a variety of devices including cell-phones, mobile computers, and TV set-top boxes.

This paper presents the initial plan for the GigaRFIC Project. The system specifications are developed in section 2. Section 3 contains the rationale for semiconductor process selection. Section 4 discusses architectures and component blocks for the receiver and transmitter. Section 5 discusses current research.

2. SYSTEM SPECIFICATIONS

The Gigabit Radio's operating specifications are different from those of conventional wireless networks. A sample set of system specifications is given in Table 1.

Table 1. Gigabit Radio system specifications

	Downlink (to Terminal)	Uplink (from Terminal)
RF Centre Frequency	17.35GHz	
Bandwidth (RF)	400MHz	
Multiple Access Scheme	TDMA	
Modulation Scheme	QAM	PSK
Duplexing Technique	TDD	TDD
Symbol Rate	400Msyms/s	400Msym/s

To achieve a high data rate, a high symbol rate must be used. The Gigabit Radio uses quadrature amplitude modulation (QAM) on its downlink at a symbol rate of 400Msym/s. The results in a very wide baseband bandwidth of 200MHz. It also requires a continuous piece of radio spectrum for transmission. The prototype Gigabit Radio uses a 400MHz band centred at 17.35GHz. This high GHz frequency is required because the required continuous bandwidth is not available in the conventional 2.4GHz or 5GHz bands. It is also required because having the system bandwidth a low percentage of the transmit frequency makes RF impedance matching easy. These wideband and high-GHz specifications are challenging constraints for RFIC and baseband design.

The simple terminal should also have low power consumption and a low bit error rate (BER). These are also challenging constraints. A general RFIC trend is that power consumption increases with operating frequency. So low power operation may be difficult. The 400MHz wide RF bandwidth increases the noise floor at the input to the receiver. In order to have a low BER, a high signal-to-noise-ratio (SNR) is required. The increased noise floor will degrade the SNR of the signal, stressing the RF link budget. These and other constraints force the designer to make a detailed analysis of all process, RF architecture, and circuit options.

3. PROCESS SELECTION

Several process technologies exist for RFIC fabrication. These include Gallium Arsenide (GaAs), Silicon CMOS, and Silicon Germanium Hetero-Junction Bipolar (SiGe HBT). Each process has both benefits and drawbacks.

GaAs is the oldest and most expensive option for RFIC fabrication. It has excellent RFIC performance since the 1980s [5]. However, digital logic is not easily integrated in GaAs and fabrication costs remain high due to the fact that it is still a specialty process. The current trend in industry is to seek

out Silicon RFIC solutions because of the potential of RF/Analog/Digital integration. As a result, GaAs was not selected for the GigaRFIC project.

Silicon CMOS is the mainstream fabrication process for digital solutions. As a result it has a lower fabrication cost due to increased economies of scale. Recently it has been used for 2GHz and 5GHz RFIC solutions [6][7], however its RFIC performance is still limited by a number of factors. These include lowered transconductance, reduced headroom and increased noise figure. The overall result is that CMOS is not the best choice for 17GHz where the system already places tight constraints on the RFIC.

Silicon bipolar technology fits somewhere between GaAs and CMOS in terms of RFIC performance. This performance is enhanced when a Germanium implant is added to the transistor base to create an HBT. The result is higher RF frequencies of operation with increased gain and reduced noise [8]. Additionally, SiGe fabrication is compatible CMOS, allow high degrees of integration. Access to IBM's 5HP SiGe BiCMOS process is currently offered through the Canadian Microelectronics Corporation (CMC). This process is the best option in terms of RF performance, integration and cost and has been selected as the fabrication option for the GigaRFIC project.

4. SYSTEM ARCHITECTURE

The next logical step after process selection and before circuit design is to analyse the potential architectures for both the transmitter and receiver based upon the system specifications. The architecture rationale for the receive path of the terminal will be presented first, followed by that for the transmit path. The envisioned block diagram for the entire transceiver is presented in Figure 2 for use as a roadmap in the discussions below.

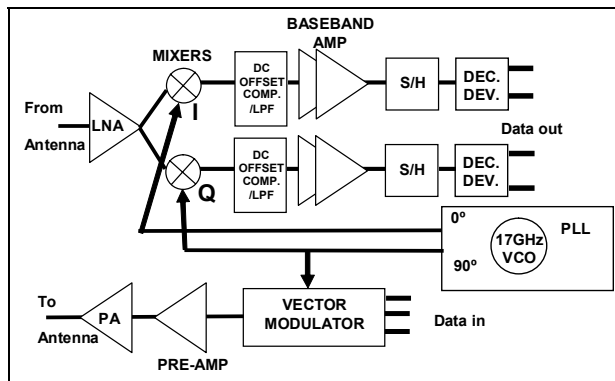


Figure 2. GigaRFIC transceiver block diagram

4.1 Receiver Architecture

The two most common architectures for RFIC receivers are super-heterodyne, and direct conversion (homodyne). The frequency diagrams for each scheme are presented in Figure 3. The following two paragraphs outline their operations.

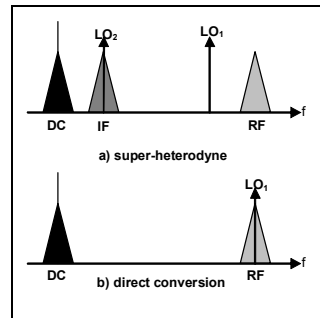


Figure 3. Frequency diagrams for super-heterodyne and direct conversion

Super-heterodyne receivers have been the traditional choice for RF receivers for the past 50 years. They have high sensitivity and selectivity, but also have drawbacks which no longer make them the automatic choice for RFIC receivers. Super-heterodyne receivers work by converting RF signals down to baseband in a series of conversion steps. Each conversion step uses a separate local oscillator (LO) tone and a mixer. The RF signal is translated down to an intermediate frequency (IF) where further amplification and filtering can occur. This partitioning of gain and filtering into different frequency bands is what gives super-heterodyne receivers their high levels of selectivity and sensitivity. However, the extra conversion stages add to system complexity and power consumption. They also have unique problems such as susceptibility to image frequencies [9].

Direct conversion receivers provide a simpler means of down-conversion. RF signals are translated down to baseband by a single conversion stage and a single LO that is at the same as the RF frequency. The single conversion stage means that the direct conversion receiver has lower complexity and power consumption. The method has existed for several decades, but was difficult to implement in board level RF systems. The technique has been re-examined for RFIC receivers because of the potential complexity and power savings [10][11].

For these reasons, the direct conversion architecture has been selected for the receive path of the Gigabit Radio terminal. However, the direct conversion receiver is not without drawbacks. The next subsection is devoted to a brief discussion of these drawbacks and how they can be mitigated within the GigaRFIC.

4.1.1 Direct Conversion Challenges

Several recent papers have been published describing the challenges of implementing a direct conversion RFIC receiver. [12][13][14][15]. The four main problems with direct conversion receivers are listed in order of severity: DC Offsets, 1/f Noise, I/Q Imbalances, and even order distortion.

The following sub-sections describe each challenge and present solutions.

4.1.1.1 DC Offsets

Most published papers refer to this as the biggest design challenge for direct conversion receivers. [13] The problem is that reverse transmission paths occur in the receiver. LO energy from the oscillator can leak through the mixer to the RF port and then re-enter the mixer. The overall effect is that the LO energy will self-mix and create a DC offset. The offset can be large enough to swamp the baseband amplifiers and destroy signal reception. This is illustrated in Figure 4.

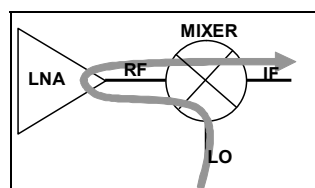


Figure 4. Illustration of LO self mixing

There are several ways to mitigate the DC offsets. The first solution is to AC-couple the baseband amplifiers to the output of the RF mixers. This has the effect of high-pass filtering the output and removing the unwanted DC-component. The challenge is that this highpass filtering also removes some signal energy and thus degrades SNR. This is less of a problem with the Gigabit Radio system since the baseband bandwidth is large when compared with traditional solutions. The second solution involves sampling the DC offset while the receiver is inactive, and subtracting the stored DC offset during reception. This requires taking the receiver off-line periodically to measure the DC offset. This is not a problem with the Gigabit Radio as it is a

TDMA system and there will be timeslots when the receiver is inactive. Therefore, the most serious direct conversion receiver challenge has two potential solutions within the Gigabit Radio system.

4.1.1.2 1/f Noise

The intrinsic noise of the baseband circuits can produce levels of noise that can reduce SNR. The RF signal only receives minimal amplification (~20dB) before being down-converted to baseband. 1/f noise is noise whose spectral profile is highest near DC. In this situation, the weak intended baseband signal can be degraded by 1/f noise of the baseband devices. However, this problem is more prominent in CMOS circuits which contain a much higher degree of 1/f noise. The choice of SiGe HBT devices for the GigaRFIC results in lower amounts of 1/f noise, and thus less signal degradation.

4.1.1.3 I/Q Imbalances

With only one frequency conversion stage, quadrature reception must be done at the RF carrier frequency. The receiver thus requires two RF mixers, one for the in-phase (I) and one for the quadrature (Q) signal component. The challenge is that imbalances in either the amplitudes or the 90° phase relationship between the I and Q paths can distort the received signal constellation. This leads to an effective reduced SNR that degrades the BER. The quadrature phase alignment is the most critical issue here. A phase difference of 6° out from 90° leads to a 2dB reduction in SNR [9].

Three potential solutions exist for I/Q imbalances. The easiest is to design a voltage controlled oscillator (VCO) with quadrature outputs. These have been implemented at lower frequencies with phase errors of less than 5° [16]. Another option would be to design a precise 90° phase shifting network. Each of these solutions would require careful and symmetric layout of the components to reduce offsets. The last solution would involve calibrating out the amplitude and phase offsets during the inactive TDMA timeslots [12]. Either the first or second solution is favoured for the GigaRFIC due to reduced complexity.

4.1.1.4 Even Order Distortion

As mentioned earlier, all RF circuits possess a certain amount of leakage. In this case leakage through the mixer from the RF port to the baseband port can lead to signal degradation. The situation occurs when two strong signals very close in frequency produce a baseband beat tone by way of non-linearities in the low-noise-amplifier (LNA) and mixer. This beat tone will

feed through the mixer and degrade the SNR of the intended signal at baseband.

Even order distortion can be reduced by making the LNA and mixer differential. This symmetry reduces all even order harmonics and distortions. So a relatively simple design fix can mitigate this source of distortion.

4.1.2 Receiver Blocks

Based upon the above discussions, some determination of the receiver block architecture can be made. See Figure 2. The LNA is implemented as a differential circuit and provides a significant amount of gain (~15dB) while operating at as low a noise figure as possible. The noise figures of the stages near the front of the radio have the greatest effect on system noise figure.

There will be two mixers in parallel after the LNA, one each for the I and Q paths. These mixers also provide gain such that some amplification of the RF signal occurs before being mixed down to baseband. The architecture of the mixer is a double-balanced Gilbert Cell [17].

Baseband amplifiers provide the balance of necessary gain such that the signal can be compared against predefined signal levels. The obvious block for this comparison is an ADC, however the wide baseband bandwidth would make its design a challenge. Fortunately, no digital signal processing is to be done at the terminal, so the ADC resolution can be reduced to simply the number of data bits required per symbol. The ADCs are now called decision devices to avoid further confusion.

4.2 Transmitter Architecture

Simplicity is again the goal for the transmit path architecture of the GigaRFIC. Structures for the RFIC blocks can be determined from system specifications in Section 2. The two most important blocks, power amplifier and vector modulator, are discussed below.

4.2.1.1 Power Amplifier

The modulation scheme on the uplink is phase-shift-keying (PSK) where a carrier's phase is modulated in accordance with the digital bits to be encoded. PSK modulation encodes no information into the amplitude of the transmitted signal. This allows a non-linear power amplifier to be used in the transmit path. Non-linear power amplifiers are more efficient than linear power amplifiers and will thus reduce the power consumption of the transmitter.

4.2.2 Vector Modulator

Transmission of digital data usually requires a DAC for the generation of analog levels for modulation purposes. This component can be simplified because of the chosen uplink modulation scheme. All that is required is a phase modulated carrier. The DAC can be replaced by a vector modulator. The function of the vector modulator is to adjust the phase of the 17GHz carrier based upon the digital levels of the current symbol. This component is simply a variable phase shift network that can be built with simple switches, identical phase shift networks, and digital logic. Similar components have been built previously at 17GHz [18].

5. CURRENT RESEARCH

Current research is focussed on developing RFIC components for the receive path of the Gigabit Radio terminal. Specifically, designs are being generated for a 17GHz differential LNA, active-mixer and LO buffer. Issues to be solved include: biasing schemes for low noise, improved circuit independence from parasitics and generation of integrated inductors at 17GHz. The design of the 400Msample/s baseband decision devices is also being investigated. Fabricated devices are expected by the middle of 2002.

These efforts seek to better understand what circuit capabilities are possible at 17GHz. With this information, the GigaRFIC RF system plans can be updated and improved.

6. CONCLUSIONS

The GigaRFIC project seeks to develop RFIC blocks for a gigabit per second wireless LAN. These RFIC blocks can be later implemented as IP cores for further SoC integration. The receive path will use a direct conversion receiver. Within the structure of the Gigabit Radio system, there exist solutions for each of the major direct conversion receiver design challenges. The transmit path will contain a vector modulator and a power efficient non-linear power amplifier. The planned fabrication process is SiGe BiCMOS that offers the benefits of both enhanced RF performance, and CMOS logic integration.

Acknowledgements

This research is supported by TRILabs, NSERC, and Alberta iCORE. Thanks are given to Stan Zwierzchowski and John M'Rory of TRILabs for their beneficial discussions. The Canadian Microelectronics Corporation is acknowledged for their technical support and fabrication services.

References

- [1] <http://www.bluetooth.org> accessed on Feb 1st, 2002.
- [2] <http://80211-planet.webopedia.com> accessed on Feb 1st, 2002
- [3] T.S. Rappaport, *Wireless Personal Communications*, Boston: Kluwer Academic, 1993.
- [4] G. M^cGibney, *Wireless Networking with Simple Terminals*, PhD Thesis, University of Calgary, 2000.
- [5] H.F. Cooke, "Microwave FETs – A Status Report", in ISSCC Dig. Tech. Papers, pp. 116-7, Feb 1978.
- [6] B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's," IEEE Journal of Solid-State Circuits, vol. 34, pp. 1382-85, October 1999.
- [7] Ting-Ping Liu, E. Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset", IEEE Journal of Solid-State Circuits, vol. 35, pp. 1927-33, December 2000.
- [8] P.R. Gray, *Analysis and Design of Analog Integrated Circuits*, New York: Wiley, 2001.
- [9] B. Razavi, *RF Microelectronics*, New Jersey: Prentice Hall, 1998.
- [10] P.M. Stroet, R. Mohindra, S. Hahn, A. Schuur, E. Riou, "A Zero-IF Single-Chip Transceiver for up to 22Mb/s QPSK 802.11b Wireless LAN" in ISSC Dig. Tech. Papers, Feb 2001.
- [11] J. Jussila, J. Ryyanen, K. Kivekas, L. Sumanen, A. Parssinen, K. Halonen, "A 22mA 3.7dB NF Direct Conversion Receiver for 3G WCDMA", in ISSC Dig. Tech. Papers, Feb 2001.
- [12] A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications", IEEE Journal of Solid-State Circuits, vol. 30, pp. 1399-1410, December 1995.
- [13] B. Razavi, "Design Considerations for Direct-Conversion Receivers", IEEE Trans. Circuits and Systems II, vol. 44, pp. 428-35, June 1997.
- [14] W. Namgoong, T.H. Meng, "Direct-Conversion RF Receiver Design", IEEE Trans. Comm., vol. 49, pp. 518-29, March 2001.
- [15] A. Mashhour, W. Domino, N. Beamish, "On the Direct Conversion Receiver – A Tutorial", Microwave Journal, pp.114-128, June 2001.
- [16] M. Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS", IEEE Journal of Solid-State Circuits, vol. 36, pp. 1025-31, July 2001.
- [17] B. Gilbert, "A precise Four-Quadrant Multiplier with Subnanosecond Response", IEEE Journal of Solid-State Circuits, vol. SC-3, pp. 365-73, December 1968.
- [18] S. Nam, A.E. Ashtiani, I.D. Robertson, "MMIC Circuits Enable Direct-Carrier Modulation", Microwaves & RF, pp. 113-125, April 1998.