

©2002 TRILabs. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from TRILabs.

Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

# The Design of a 17.35 GHz LNA and Mixer

Michael W. Lynch, J.W. Haslett  
TRLabs / University of Calgary  
Suite 280, 3553 31<sup>st</sup> Street N.W.  
Calgary, Alberta Canada. T2L 2K7  
mlynch@cal.trlabs.ca, haslett@enel.ucalgary.ca

*Abstract*— The performance of radio-frequency integrated circuit (RFIC) blocks such as low noise amplifiers (LNA) or mixers is enhanced by achieving a simultaneous noise and power match at the input. This paper presents a design strategy for achieving this match for circuits built from bipolar transistors with inductive degeneration. The strategy is applied to the design of a 17.35 GHz LNA and a 17.35 GHz direct down-conversion mixer. Simulated results with extracted parasitics show a simultaneous noise and power match for both the LNA and mixer. The results for these two components are compared with those previously published by other authors.

## I. INTRODUCTION

“Wireless” has promised and delivered the ability to connect to other devices, users and networks at anytime and anywhere. However, “Wireless” has not yet delivered that connectivity at very high data rates. Current wired and optical data rates are in the gigabit-per-second range, while current and up-coming wireless protocols deliver connection rates that are at best in the 10’s of megabits-per-second range. Figure 1 gives an overview of various connection rates for cellular, wireless local area networks, and personal area networks. [1], [2], [3]

The Gigabit Radio is a prototype 4th generation wireless local area network being developed by researchers at TR Labs. One of its goals is to vastly improve wireless network data rates. Researchers at TR Labs and the University of Calgary have also started the GigaRFIC project. Its goal is to create radio-frequency integrated circuit (RFIC) components for the Gigabit Radio terminals. The long term goal is to integrate these RFIC components, along with the

This work is supported by NSERC ([www.nserc.ca](http://www.nserc.ca)), iCORE ([www.icore.ca](http://www.icore.ca)), and TR Labs ([www.trlabs.ca](http://www.trlabs.ca)). The Canadian Microelectronics Corporation ([www.cmc.ca](http://www.cmc.ca)) is acknowledged for technical support and access to leading semiconductor manufacturing processes.

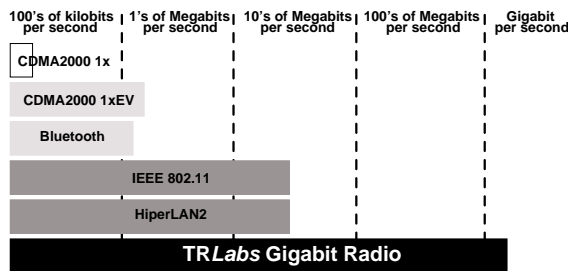


Fig. 1. Wireless Data Rate Comparison Chart

baseband and digital logic blocks, to create a transceiver-on-a-chip.

This paper is organized as follows. Section II will outline system aspects of the Gigabit Radio system that affect the design of the GigaRFIC terminal components. Section III will contain an analysis of the simultaneous noise and power matching problem for bipolar transistors. A strategy for achieving this optimum condition will then be presented. Section IV will present the design of a 17.35 GHz low noise amplifier (LNA). Simulated results will be presented and compared with previously published works. Section V will present the design of a 17.35 GHz down-conversion mixer. Simulated results will again be presented and compared with previous works. Finally, Section VI will present conclusions and directions for future research.

## II. SYSTEM ASPECTS

The Gigabit Radio system has many differences from conventional wireless networks, such as its high frequency of operation. However, it also shares some requirements with conventional wireless systems, such as low power consumption. Several choices have been made at the system level that must be discussed so that the design constraints on the GigaRFIC components can be understood.

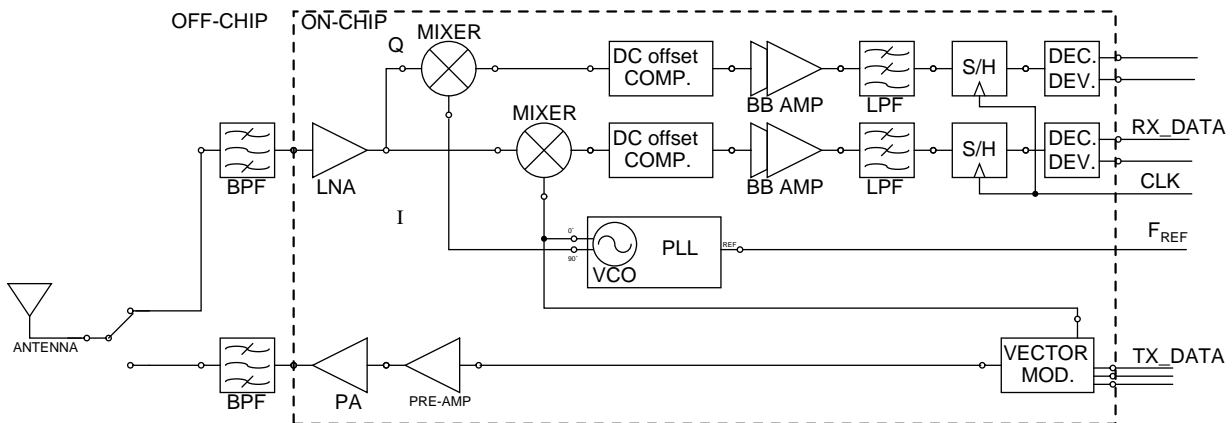


Fig. 2. GigaRFIC System Block Diagram

### A. High GHz Operation

While conventional wireless LANs operate at frequencies in the 2.4 GHz and 5 GHz bands, the Gigabit Radio system operates at 17.35 GHz. The system requires 400 MHz of continuous spectrum that cannot be found in lower frequency ranges. This requirement of high-GHz operation is a unique design constraint under which the GigaRFIC components must be designed. To achieve reasonable performance at 17.35 GHz, a SiGe BiCMOS process ( $f_T \approx 50$  GHz) was selected for RFIC implementation.

### B. Low Bit Error Rate

The Gigabit Radio system also targets very low bit error rates for wireless transmission. The 400 MHz of input channel bandwidth raises the receiver noise floor significantly, making this difficult to achieve. A potential solution to this problem is to increase the transmitted power, but this can only be done to a certain extent. As a result, the RFIC blocks must also be designed to minimize the total receiver noise figure. Basic system theory [4] shows that noise figure for a series of cascaded blocks is

$$NF_{sys} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \dots \quad (1)$$

This illustrates that the system noise figure is strongly influenced by the noise figure and gain of the first blocks in the chain. This necessitates an LNA and a mixer with high gains and low noise figures.

### C. Low Power

Since the terminal devices will be wireless, they will also be battery powered. This means that RFIC blocks must also be designed with power consumption minimized.

The block diagram for the GigaRFIC transceiver is shown in Figure 2. The receiver is a direct conversion receiver that minimizes the number of RFIC blocks and external components. This will reduce system complexity and power consumption. Direct conversion transceivers have several design implementation issues that will not be discussed here. The interested reader is referred to [5], [6], [7] for those issues and their solutions. Direct conversion transceivers are a current industry trend with several systems having recently been implemented. [8], [9], [10]

## III. SIMULTANEOUS NOISE AND POWER MATCHING

As mentioned in Section II, in order to achieve low bit error rates, the noise figure of the system must be minimized so that sufficient SNR remains at the output of the receiver for low bit error rate communications. Equation (1) shows that both the gain and noise figure of the LNA have a strong effect on the overall receiver noise figure. The LNA must be designed with these two parameters in mind. The mixer is the second block in the receiver chain and its noise figure and gain will also have some effect on the total system noise figure. A design strategy to address these issues will be developed in this section.

### A. Optimum Source Admittance

The development of this strategy begins with an analysis of the noise properties of a BJT in common-emitter configuration. Classical two-port noise theory allows all of the inherent noise sources to be amalgamated into two noise sources, an input referred noise current and an input referred noise voltage, that are then placed in front of the now noiseless transistor. This situation is illustrated in Figure 3.

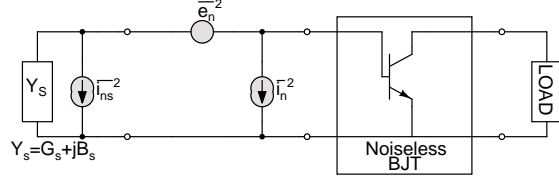


Fig. 3. Two-port network with noise sources input referred

The noise figure of a two port network, with its noise sources input referred is a function of its source admittance ( $Y_s = G_s + jB_s$ ). The noise figure of this two port can be minimized by selecting an optimum source admittance ( $Y_{s_{opt}} = G_{s_{opt}} + jB_{s_{opt}}$ ). This  $NF_{min}$  and optimum source admittance are then found to be:

$$NF_{min} = 1 + 2(C_r + \sqrt{R_n G_n - C_i^2}) \quad (2)$$

$$G_{s_{opt}} = \sqrt{\frac{G_n}{R_n} - \left(\frac{C_i}{R_n}\right)^2} \quad (3)$$

$$B_{s_{opt}} = \frac{C_i}{R_n} \quad (4)$$

where

$R_n = \frac{e_n^2}{4kT\Delta f}$  is the equivalent noise resistance.

$G_n = \frac{i_n^2}{4kT\Delta f}$ ; is the equivalent noise conductance

$C_r = \frac{\Re\{\epsilon_n i_n^*\}}{4kT\Delta f}$ ; is the real part of the correlation between the input referred noise sources.

$C_i = \frac{\Im\{\epsilon_n i_n^*\}}{4kT\Delta f}$ ; is the imaginary part of the correlation between the input referred noise sources.

Several authors have derived equations for the  $NF_{min}$  of a bipolar transistor based upon small signal and DC parameters. [11], [12], [13], [14] This leads to the fact that  $Y_{s_{opt}}$  can be manipulated by changing transistor dimensions and bias currents. Specifically, an RFIC designer has control over the emitter length,  $l_{emitter}$ , and collector current,  $I_C$ .

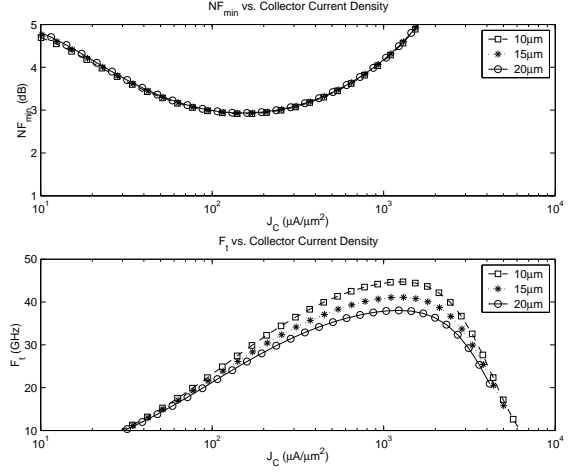


Fig. 4.  $NF_{min}$  and  $f_T$  vs.  $J_{C_{opt}}$  for various emitter lengths

### B. Optimum Collector Current Density

In addition to minimizing the noise figure by providing  $Y_{in} = Y_{s_{opt}}$ , it is possible to further minimize  $NF_{min}$  by selecting the proper collector current density ( $J_{C_{opt}}$ ). [11] first identified that  $NF_{min}$  depended upon  $I_C$  and [14] further elaborated upon the fact that  $NF_{min}$  is in fact dependent upon  $J_{C_{opt}}$ . To quickly verify this, a sweep was done with a SiGe transistor in the Cadence simulator to produce Figure 4. An interesting trade-off is illustrated in Figure 4: collector current biasing for low noise decreases the transistor  $f_T$ . Thus for a given  $f_T$ , low noise operation becomes difficult as frequencies increase.

### C. Inductive Degeneration

Power transfer into a device can be maximized by having the device input admittance  $Y_{in}$  match the conjugate of the source admittance  $Y_s$ . This is one very important factor in maximizing the gain through the two-port. However, the power matching admittance is not necessarily the same as the  $Y_{s_{opt}}$  described in Section III-A.

To achieve greater design flexibility over common emitter input admittance, a technique called inductive degeneration is employed. Figure 5 shows the complete small signal model of the BJT with a degeneration inductor placed at the emitter terminal. Ignoring all noise sources (shown in grey) in Figure 5 for the moment, the



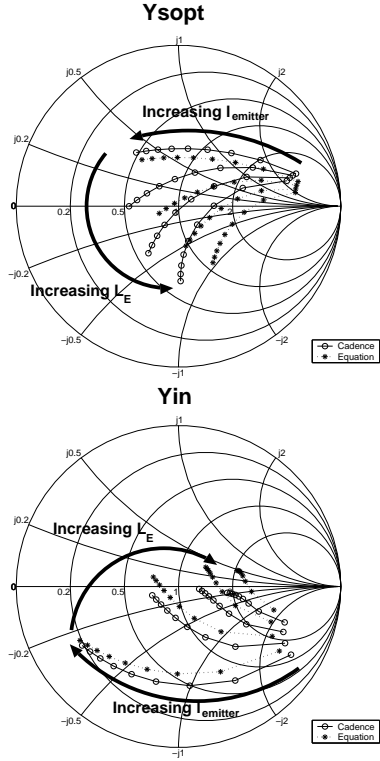


Fig. 6. Comparison of simulation and equation based  $Y_{in}$  and  $Y_{s_{opt}}$

form an L-matching network to transform the off-chip  $50\Omega$  impedance into the simultaneous optimum impedance for noise and power matching.

#### IV. LNA DESIGN

The LNA schematic is shown in Figure 8. It is a two stage design featuring a common emitter first stage and a cascode configuration second stage. Biasing details are omitted from the schematic, however both stages are biased at the  $J_{C_{opt}}$  for Q1 and Q2. All inductors are on-chip planar spiral inductors constructed from  $2\mu\text{m}$  thick top level metal.

The first stage of the LNA consists of a single transistor Q1 biased at its optimum collector current density. The emitter length is sized in conjunction with the inductance of spiral inductor  $L_E$  such that the Q1's  $Y_{s_{opt}}$  is equal to  $Y_{in}^*$ . Spiral inductor  $L_B$  and shunt parasitic pad capacitance ( $\approx 90\text{fF}$ ) are used to impedance match the input of the first stage to  $50\Omega$ . Because of

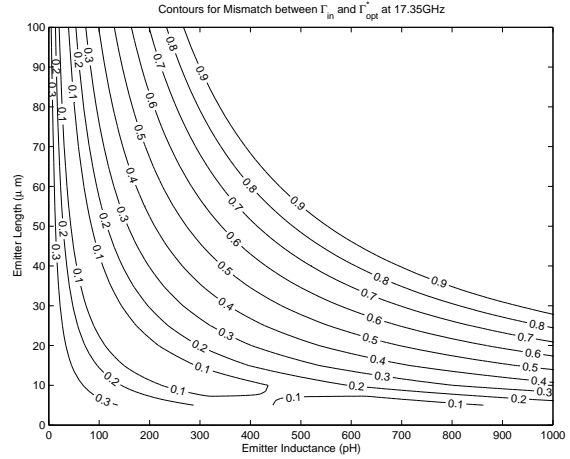


Fig. 7. Contour plot of (14) in  $l_{emitter} - L_E$  space

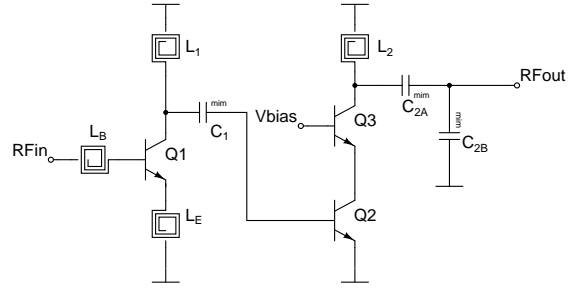


Fig. 8. LNA Schematic

$L_E$ , the  $g_m$  and hence the gain of this stage are degenerated. As such, it is necessary to add a second stage to the LNA to increase the gain.

The second stage is made up of transistors Q2 and Q3 in a cascode configuration. No emitter inductor is used on Q2 so as to keep the gain of this stage un-degenerated and thus high. Q2 is still biased at its  $J_{C_{opt}}$ .  $L_1$  and  $C_1$  form an L-match between the first and second stages of the LNA. These elements provide an impedance to Q2 that is a compromise between one that maximizes second stage gain and one that minimizes the noise figure of the second stage. Q3 was sized smaller than Q2 in order to boost its  $f_T$ . The on-chip spiral inductor  $L_2$  and capacitors  $C_{2A}$  and  $C_{2B}$  form a three element match that matches the output of the LNA to  $50\Omega$  for testing purposes.

A layout was generated for the LNA; it is shown in Figure 9. Care was taken to minimize layout area and trace lengths while still maintaining minimum separation distances between spiral

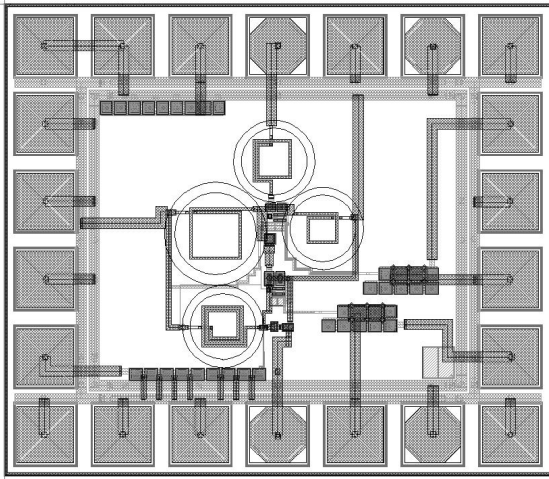


Fig. 9. LNA Layout

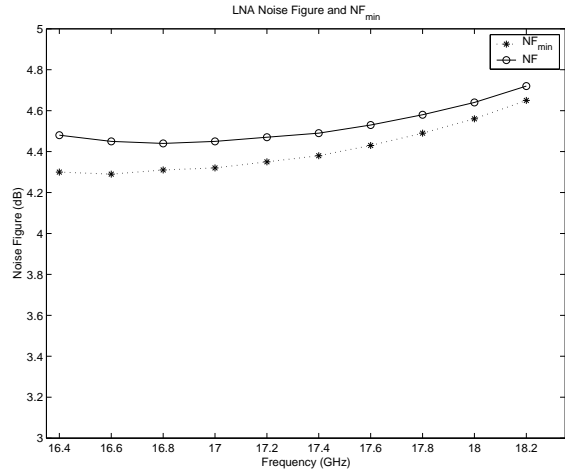


Fig. 11. LNA  $NF$  and  $NF_{min}$

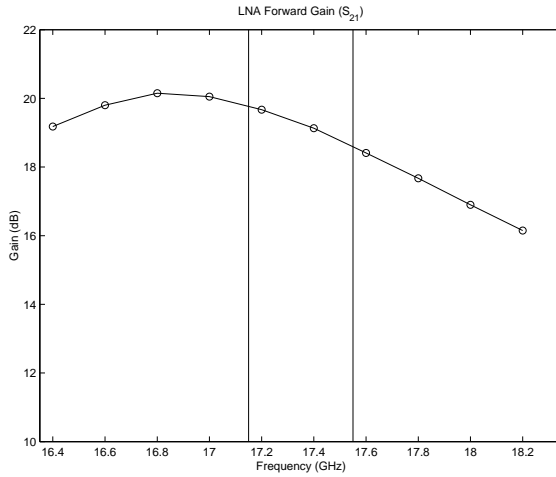


Fig. 10. LNA Gain

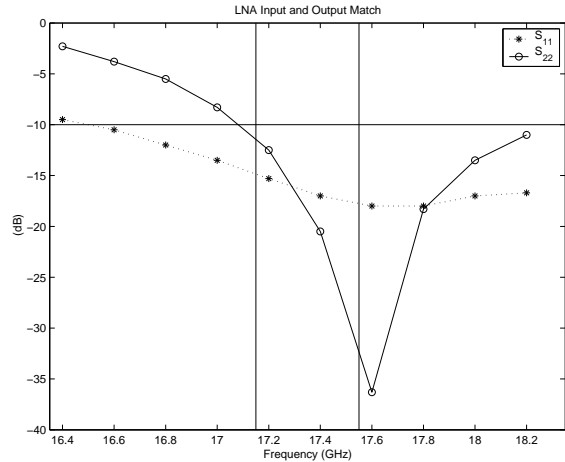


Fig. 12. LNA Input and Output Match (dB)

inductors of at least  $80\mu\text{m}$ . The layout including pads occupies an area of  $910\mu\text{m} \times 1060\mu\text{m}$ .

Parasitics were extracted from the layout and added to the simulation netlist. Simulated results including all layout parasitics are shown below. Figure 10 shows a simulated forward gain of 19.2 dB. Figure 11 shows that simulated noise figure of the LNA is 4.5dB, just 0.1dB above the  $NF_{min}$  for the LNA.  $S_{11}$  and  $S_{22}$  are plotted in Figure 12. Both are below -10dB across the system bandwidth. A simultaneous noise and power match has been achieved. The LNA is biased with 4.5mA from a 3.3V power supply.

This 17.35 GHz LNA is compared with other high-GHz RFIC LNAs in Table I. This LNA

provides an amount of gain that is comparable with [15]. The simulated noise figure matches well with other LNAs operating at 15 GHz and above. Note that higher  $f_T$  processes can achieve lower noise figures as the operating frequency is farther away from  $f_T$ . This explains the slightly better noise performance in [15] and in the 6 GHz LNAs such as [16].

Source	Technology	Frequency (GHz)	$S_{11}$ (dB)	Gain (dB)	$S_{22}$ (dB)	Noise Figure (dB)
[16]	SiGe ( $f_T=40$ GHz)	6.00	-12	16.0	-12	1.9
[17]	SiGe ( $f_T=80$ GHz)	6.20		31.0		1.3
[17]	Si ( $f_T=52$ GHz)	9.50		21.0		2.8
[17]	SiGe ( $f_T=80$ GHz)	10.50		26.0		2.0
[18]	SiGe ( $f_T=80$ GHz)	15.00	-10	12.0		4.0
[15]	SiGe ( $f_T=90$ GHz)	23.00		21.0		4.1
<b>This Work</b>	SiGe ( $f_T=50$ GHz)	17.35	-18	19.5	-14	4.5

TABLE I  
COMPARISON WITH LNAs FROM PREVIOUS WORKS

## V. MIXER DESIGN

The schematic for the mixer core is shown in Figure 13. It is a fully balanced mixer with differential inputs (RF and LO), and outputs. DC bias circuitry has been omitted for clarity. On-chip passives  $L_{tank}$  and  $C_{tank}$  form a resonant tank that resonates at the RF frequency (17.35 GHz). Transistors Q1 and Q2 make up the Gm-pair that converts the applied RF voltage signal to an RF current. That current is fed into the tails of two emitter coupled pairs (Q3-Q4 and Q5-Q6). These four transistors make up the mixing quad. Its function is to switch the RF current across two loads in response to an applied differential LO voltage. The loads for the mixer are resistive loads because the mixer is intended for direct down-conversion as described Section II-C.

The design of the GM-pair within the mixer core borrows heavily on the design strategy developed for the LNA. Again, Q1 and Q2 are biased at their  $J_{C_{opt}}$  to minimize their noise figures. Emitter lengths and emitter degeneration inductors are sized to achieve simultaneous noise and power match at the input.

The mixing quad consisting of Q3-Q6 is designed to behave as closely to an ideal switch as possible at 17.35 GHz. Q3-Q6 are sized smaller than Q1-Q2 such that their  $f_T$  are maximized. Switching noise is transferred to the mixer output at the instants where both sides of the mixing quad are “on”. By maximizing the  $f_T$ ’s of the mixing quad transistors, more ideal switching and thus a lower noise figure results. [19]

Additional circuitry to facilitate testing was included on-chip. The LO buffer in Figure 14 is

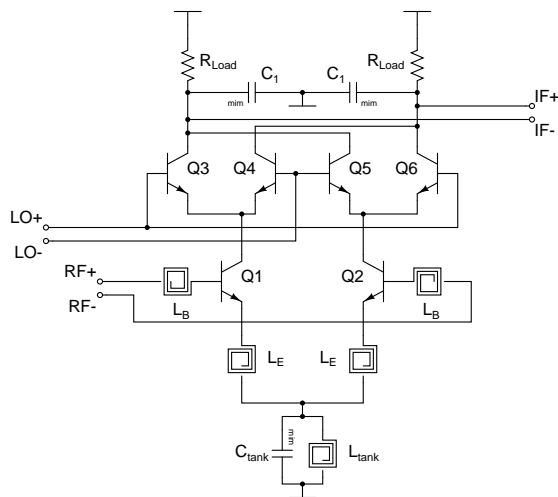


Fig. 13. Mixer schematic

simply an active balun that takes a single-ended LO test signal and converts it to a  $400mV_{p-p}$  differential signal that is then applied to the LO inputs of the mixing quad. At the output, the baseband signal needs to be converted from double-ended to single ended. This is done with the baseband amplifier which is another active balun. The baseband amplifier is designed to match the output to  $50\Omega$  and to provide  $\approx 9dB$  of gain to counter the 6dB loss incurred from going to a single-ended signal. The baseband amplifier is shown in Figure 15.

The layout for the mixer test chip is shown in Figure 16. The chip utilizes the same  $910\mu m \times 1060\mu m$  pad frame as the LNA for ease of test. Great attention was paid to symmetrical layout as most circuits are differential. The layout was also made as compact as possible to minimize

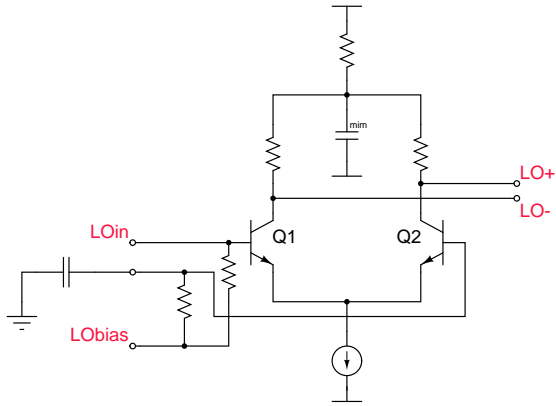


Fig. 14. Local Oscillator Buffer

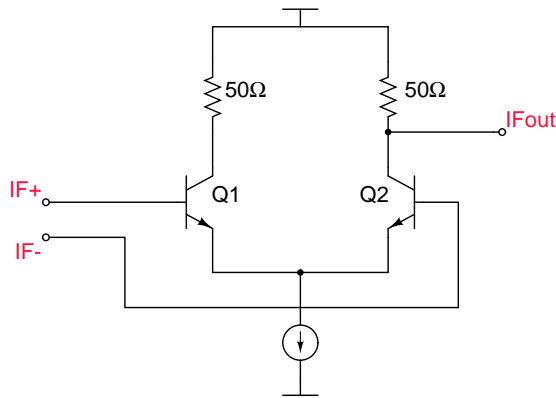


Fig. 15. Mixer Output Amplifier

parasitics while still maintaining a minimum inductor spacing of  $80\mu\text{m}$ .

Parasitics were extracted from the layout and included in the simulation netlist. The simulated noise figure and  $NF_{min}$  are presented in Figure 17. The single sideband (SSB) noise figure is less than 0.3dB above the SSB  $NF_{min}$ . However, as this is a down conversion mixer intended for direct conversion, the double sideband (DSB) noise figure is the more appropriate measure. Therefore the noise figure for the mixer test block is 10.8dB. Input return loss ( $S_{11}$ ) is plotted in Figure 18. A good input match is achieved across the system band. The mixer is simultaneously noise and power matched. Conversion gain from 17.35 GHz down to DC is also plotted in Figure 18. The conversion gain for the mixer test block is 12.7dB. The mixer core is biased with 5.4mA of current from a 3.3V supply.

A literature search for RFIC mixers targeting

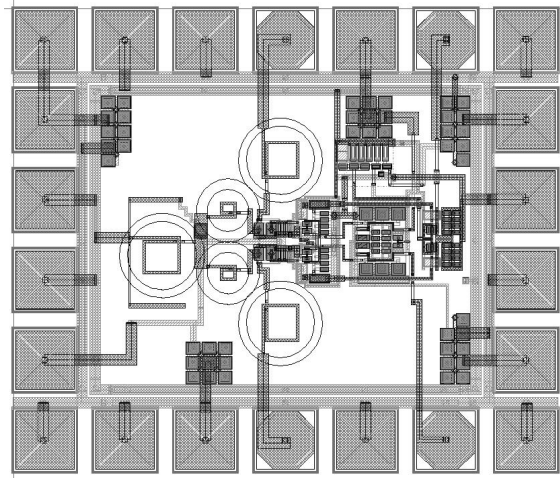


Fig. 16. Mixer Layout

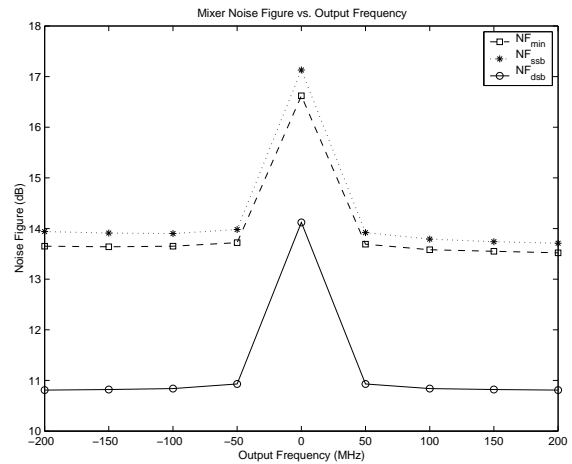


Fig. 17. Mixer Noise Figure

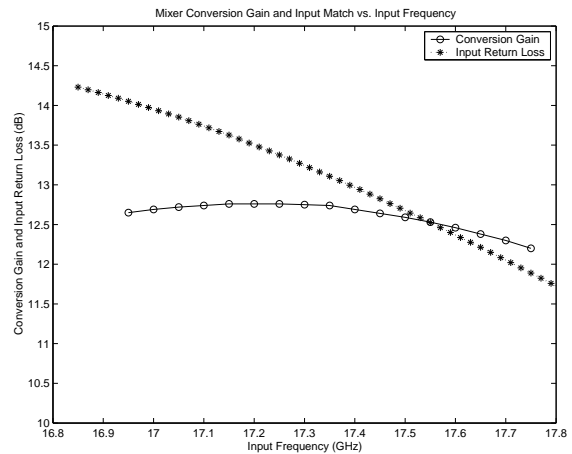


Fig. 18. Mixer Conversion Gain and Input Return Loss

Source	Technology	Frequency (GHz)	IF (GHz)	Gain (dB)	IIP3 (dBm)	Noise Figure DSB (dB)
[20]	SiGe ( $f_T=50$ GHz)	11.2	1.25	16.1	.	9.4
[21]	Si ( $f_T=50$ GHz)	17.0	0.24	5.4	-9.9	8.8
[21]	SiGe ( $f_T=80$ GHz)	20.0	0.24	10.0	-11.3	6.0
[22]	SiGe ( $f_T=50$ GHz)	20.0	1.00	10.0	-1.0	17.0
[23]	SiGe ( $f_T=80$ GHz)	30.0	0.30	5.9	.	10.0
<b>This Work</b>	SiGe ( $f_T=50$ GHz)	17.35	0.00	12.7	-14.0	10.8

TABLE II  
COMPARISON WITH MIXERS FROM PREVIOUS WORKS

operation above 10 GHz was performed. The results, along with the simulated results for this mixer are presented in Table II. This mixer achieves good performance in terms of gain and noise figure with a relatively low  $f_T$  process.

## VI. CONCLUSIONS AND FUTURE WORK

This paper has presented a simultaneous noise and power matching strategy for bipolar transistors utilizing inductive degeneration. It matches the transistor's arbitrary  $Y_{s_{opt}}$  to  $Y_{in}$  by adjusting  $l_{emitter}$  and  $L_E$ . The technique was employed in the design of a 17.35 GHz LNA. The LNA achieved simulated gain and noise figure of 19dB and 4.5dB respectively. The noise and power match strategy was also employed in the design of a direct down-conversion 17.35 GHz fully balanced mixer. The mixer achieved a simulated conversion gain of 12.7dB and a DSB noise figure of 10.8dB. These results are achieved with a relatively low  $f_T$  fabrication process.

Future work on the GigaRFIC project will involve testing the LNA and mixer. Fabricated devices are expected back in the last half of 2002. These devices will be tested with on-chip wafer probes, and with a flip-chip packaging technique. Future GigaRFIC blocks such as the VCO and PLL are being developed by other researchers at TRILabs and the University of Calgary.

## REFERENCES

- [1] "http://80211-planet.webopedia.com," accessed, May 2002.
- [2] "http://www.cdma.com/cdma/3g.html," accessed, May 2002.
- [3] "http://www.bluetooth.com," accessed, May 2002.
- [4] George D. Vendelin, *Design of Amplifiers and Oscillators*, John Wiley & Sons, New York, 1982.
- [5] Asad A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1415, Dec. 1995.
- [6] Behzad Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II*, vol. 44, no. 6, pp. 428–435, June 1997.
- [7] Won Namgoong and Teresa H. Meng, "Direct conversion RF receiver design," *IEEE Transactions on Communications*, vol. 49, no. 3, pp. 518–529, Mar. 2001.
- [8] Peter M. Stroet, Rishi Mohindra, Steffen Hahn, Axel Schuur, and Emmanuel Riou, "A zero-IF single-chip transceiver for up to 22Mbps QPSK 802.11b wireless LAN," in *ISSCC Digest of Technical Papers*, Feb. 2001.
- [9] Ting-Ping Liu and Eric Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1927–1933, Dec. 2000.
- [10] Behzad Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1382–1385, Oct. 1999.
- [11] H. Fukui, "The noise performance of microwave transistors," *IEEE Transactions on Electron Devices*, vol. ED-13, no. 3, pp. 329–341, Mar. 1966.
- [12] Laurent Escotte, Jean-Phillipe Roux, Robert Plana, Jacques Graffeuil, and Andreas Gruhle, "Noise modeling of microwave heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 42, no. 5, pp. 883–889, May 1995.
- [13] Sorin P. Voinigescu, Michael C. Maliepaard, Jonathan L. Showell, Greg E. Babcock, David Marchesan, Michael Schroter, Peter Schvan, and David L. Harame, "A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1430–1439, Sept. 1997.
- [14] Osama Shana'a, Ivan Linscott, and Len Tyler, "Frequency-scalable SiGe bipolar RF front-end design," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 888–895, June 2001.
- [15] Gerd Schuppener, Takashi Harada, and Yinggang Li, "A 23-GHz low-noise amplifier in SiGe heterojunction bipolar technology," in *IEEE RFIC Symposium Digest of Papers*, 2001.
- [16] J. Sadowy, J. Graffeuil, E. Tournier, L. Escotte, and R. Plana, "Advanced design of high linearity, low noise amplifier for WLAN using SiGe BiCMOS tech-

- nology," in *2001 Topical Meeting on Silicon Monolithic Integrated Circuits*, 2001, pp. 6–11.
- [17] Dietmar Zoschg, Wilhelm Wilhelm, Herbert Knapp, Klaus Aufinger, Josef Bock, T. F. Meister, Martin Wurzer, Hans-Dieter Wohlmuth, and Arpad L. Scholtz, "Monolithic low-noise amplifiers up to 10-GHz in Silicon and SiGe bipolar technologies," in *Proceedings of the 30th European Microwave Conference*, 2001, pp. 332–5.
- [18] Herbert Knapp, Dietmar Zoschg, Thomas Meister, Klaus Aufinger, Sabine Boguth, and Ludwig Treitinger, "15-GHz wideband amplifier with 2.8dB noise figure in SiGe] bipolar technology," in *IEEE RFIC Symposium Digest of Papers*, 2001.
- [19] Sorin P. Voinigescu and michael C. Maliepaard, "5.8GHz and 12.6GHz Si bipolar MMICs," in *ISSCC Digest of Technical Papers*, Feb. 1997.
- [20] W. Durr, U. Erber adn A. Schuppen, H. Dietrich, and H. Schumacher, "Low-power low-noise active mixers for 5.7 and 11.2-GHz using commercially available SiGe HBT MMIC technology," *Electronics Letters*, vol. 34, no. 21, pp. 1994–1996, Oct. 1998.
- [21] Sabine Hackl, Martin Wurzer, Josef Bock, Thomas F. Meister, Herbert Knapp, Klaus Aufinger, Sabine Boguth, Ludwig Treitinger, and Arpad L. Scholtz, "Benefits of SiGe over silicon bipolar technology for broadband mixers with bandwidth above 10GHz.," in *IEEE RFIC Symposium Digest of Papers*, June 2001.
- [22] K.B. Schad, H. Schumacher, and A. Schuppen, "Low-power active mixer for Ku-band application using SiGe HBT MMIC technology," in *IEEE International Microwave Symposium Digest*, June 2000.
- [23] Sabine Hackl, Herbert Knapp, and Ludwig Treitinger, "30-GHz active mixer in a Si/SiGe bipolar technology," in *Proceedings of 2000 Asia-Pacific Microwave Conference*, 2000, pp. 780–782.