The Design of a 17.35GHz LNA and Mixer

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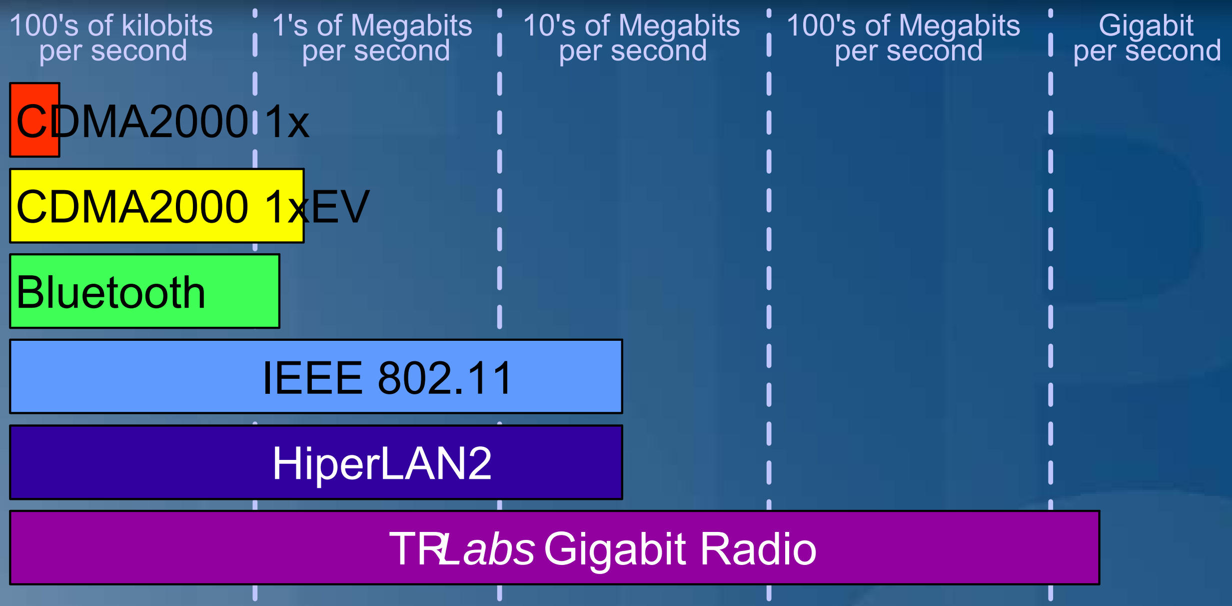
Outline

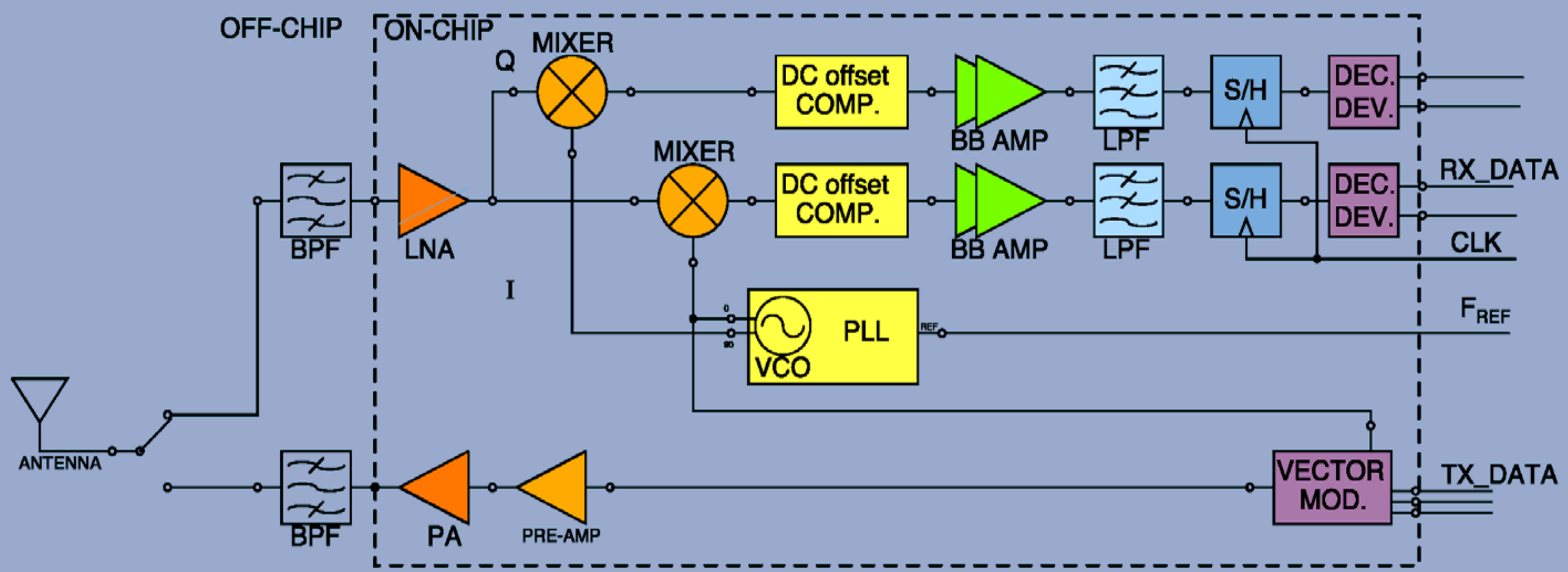
- Introduction - What is GigaRFIC?
- Low Noise Biasing Theory
- LNA Design and Results
- Mixer Design and Results
- Summary and Future Work

The Wireless "Bottleneck"



- Current wireless data rates limited to 10's of MBps
- TRLabs Gigabit Radio is a prototype 4th generation wireless network
- Uses advanced DSP techniques at the basestation to achieve data rates in excess of 1 GBps
- Gigabit Terminals are simpler devices with no heavy DSP

The GigaRFIC Terminal



GigaRFIC Design Considerations

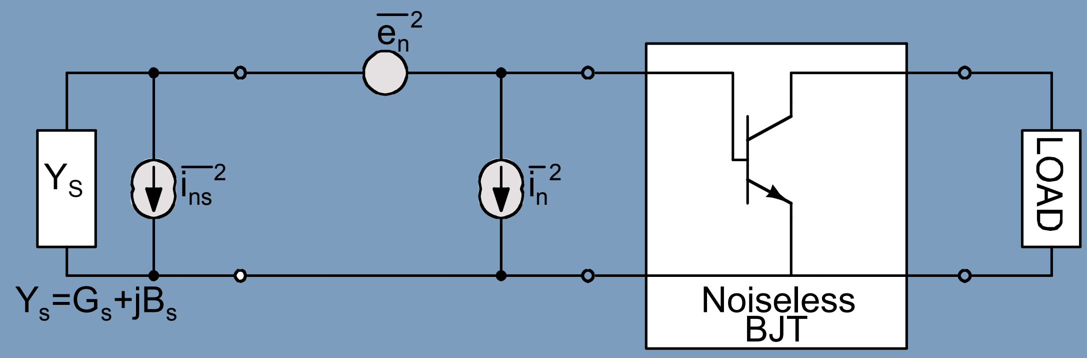
- High GHz Operation - 17.35GHz
  - 400MHz of RF channel bandwidth
- Wide Channel Bandwidth
  - Baseband circuitry requires wide bandwidths
  - Raises input noise floor
- Low Bit Error Rate
- Simplicity of architecture

Low Noise Biasing

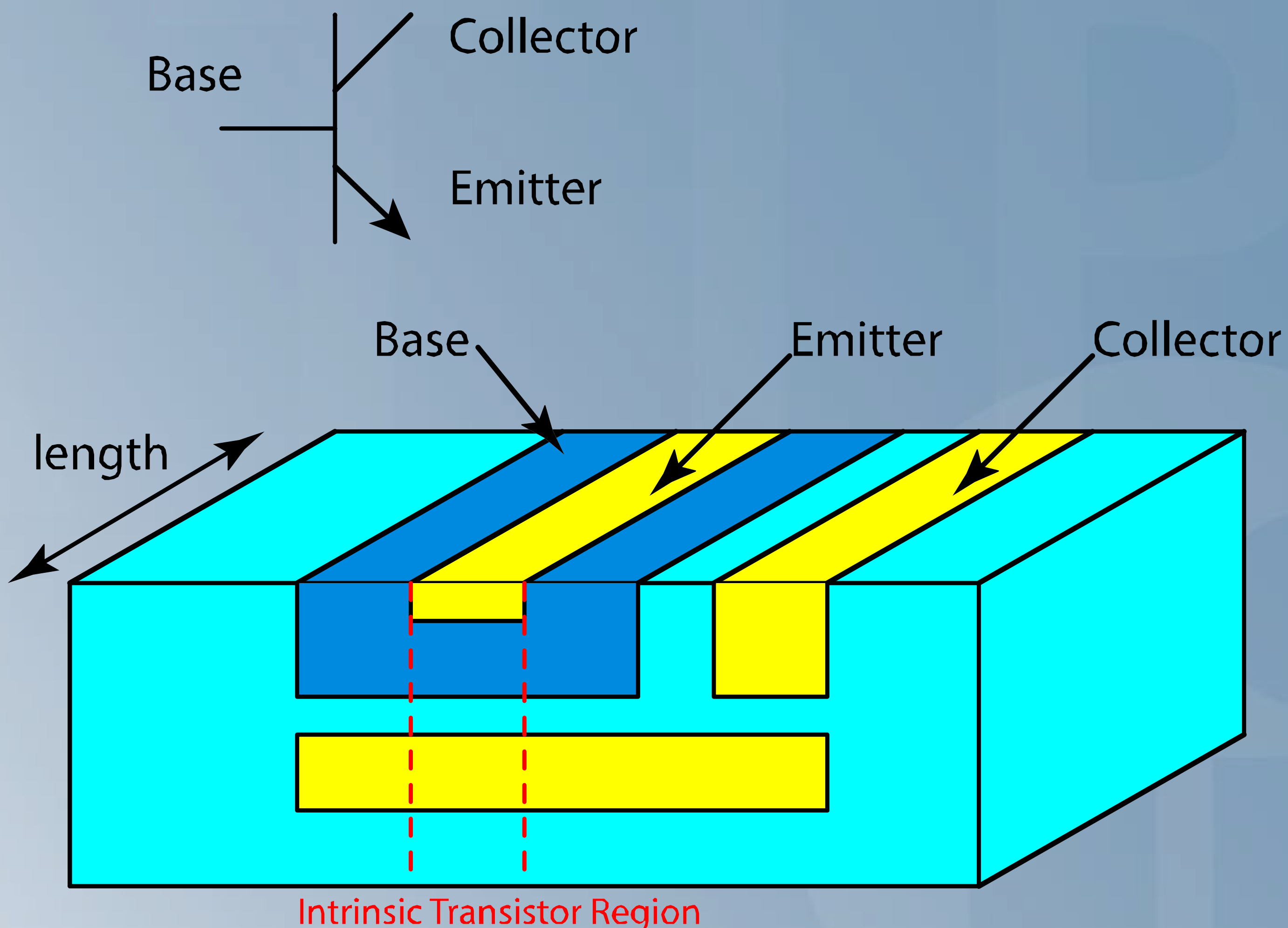
- To minimize receiver noise figure, initial stages must be low noise
  - LNA
  - Mixer
- A low noise biasing technique is important in the design of both blocks

Optimum Source Admittance (Y_{Sopt})

- Noise figure is the amount of SNR degradation through a block
- Noise theory allows noise sources to be input referred
  - e_n^2, i_n^2
- From these input noise sources, an optimum source admittance (**Y_{Sopt}**) that minimizes the noise figure can be found.
- This achieves the minimum noise figure (**NF_{min}**)
- **Y_{Sopt}** is a function of transistor geometry, bias current,…
- Emitter length (**$l_{emitter}$**)

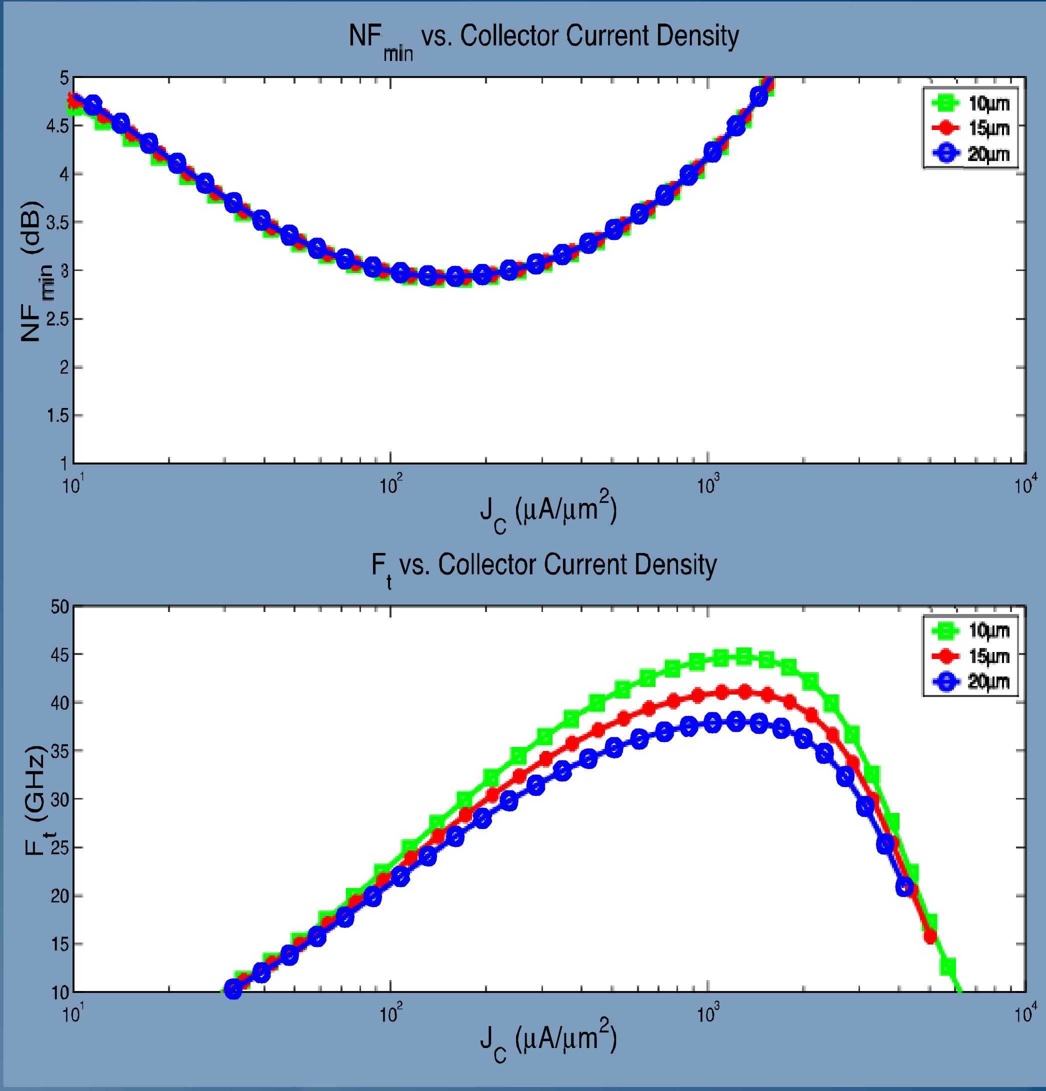


Transistor Geometry



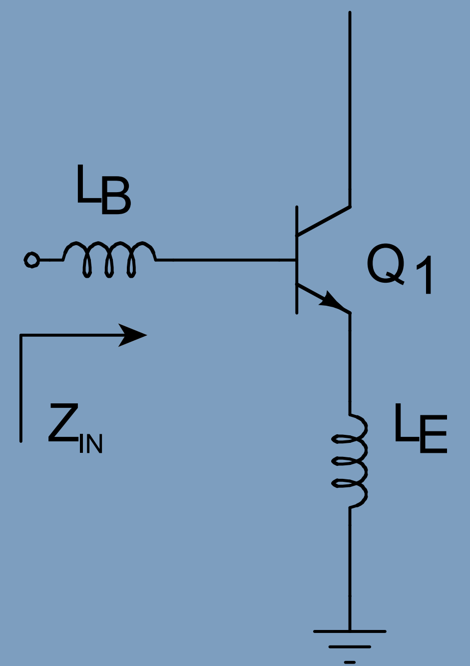
Minimizing NF_{min}

- NF_{min} is a function of collector current density (J_{Copt})
- Balancing of BJT noise sources
- Geometry independent
- Lowers f_T



Inductive Degeneration

- Power matching
- Use L_E to set real part of Z_{IN} to 50Ω.
- Use L_B to set imaginary part to zero
- Drawback: Reduced gain



$$Z_{IN} = s\cdot(L_E + L_B) + \frac{1}{s\cdot C_\pi} + \frac{g_m \cdot L_E}{C_\pi}$$

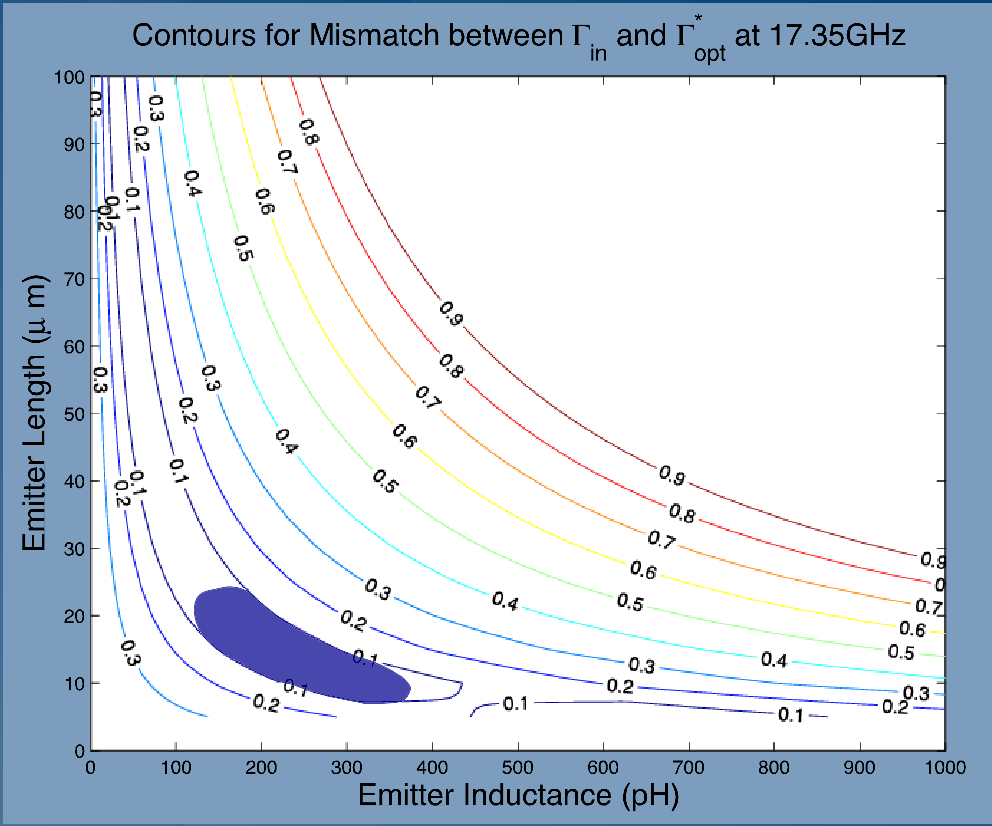
Design Strategy

- Designer has several variables
  - $I_{emitter}$, J_{Copt}, L_E, L_B

1. Use J_{Copt} to minimize NF_{min}
2. Use L_E and $I_{emitter}$ to make

   $$Z_{IN} = Z_{Sopt}^{*}$$

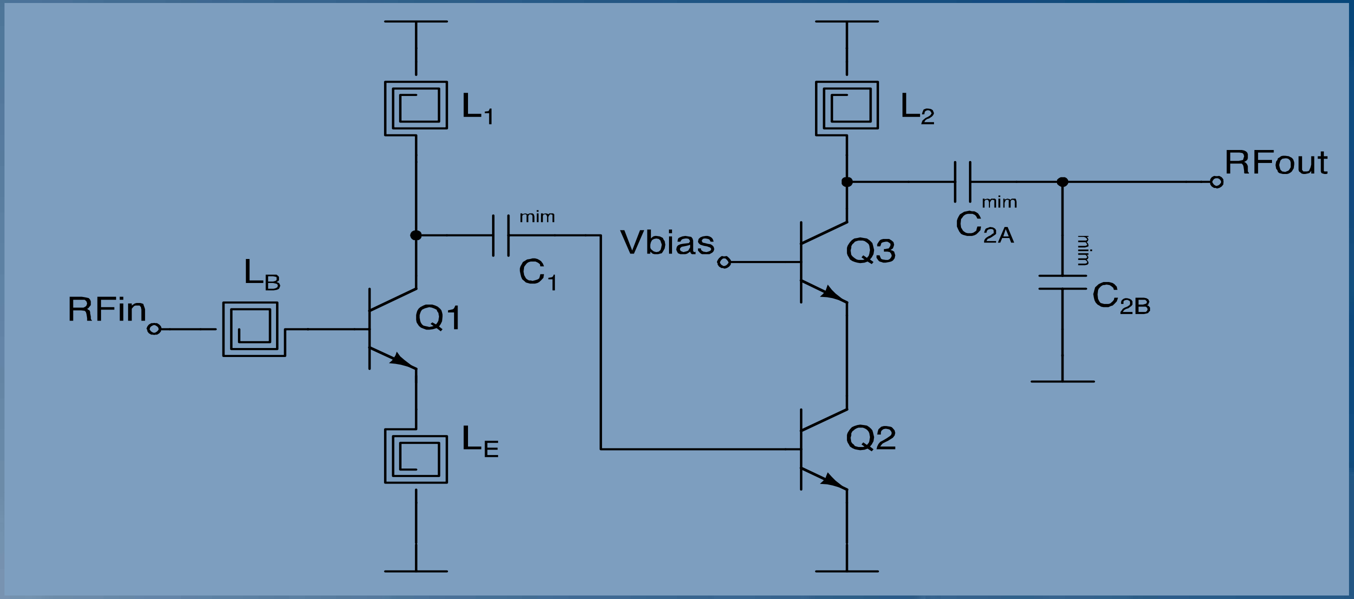
3. Use L_B and bondpad capacitance to match to 50Ω



$$mismatch = \left|\frac{Z_{s_{opt}} - Z_{in}^{*}}{Z_{s_{opt}} + Z_{in}^{*}}\right| \leq 1.$$

LNA Design and Results

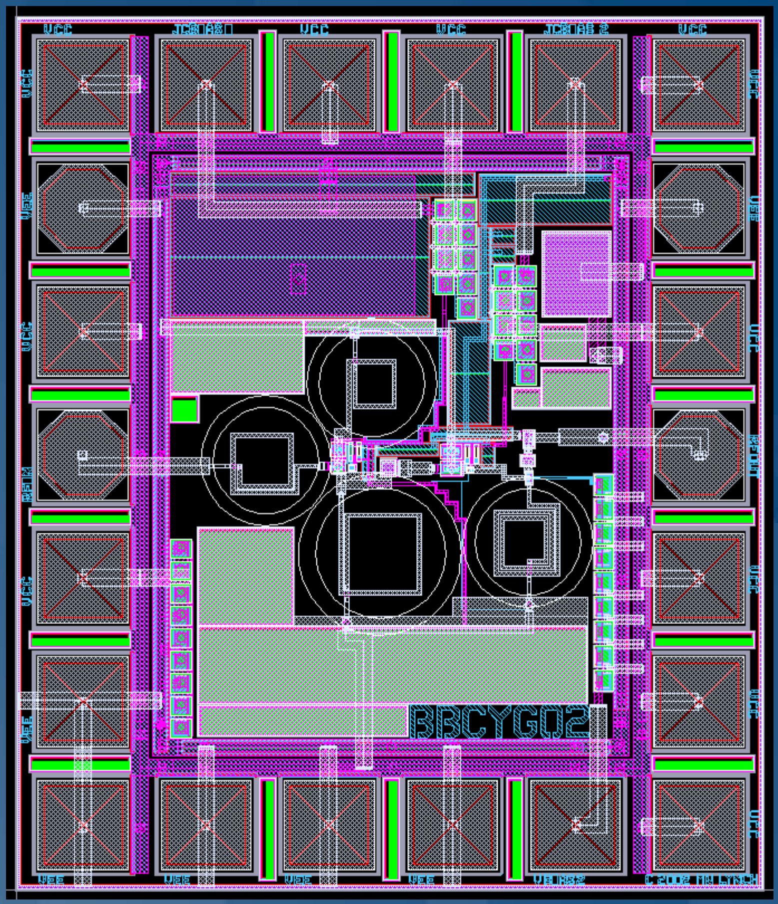
LNA Schematic



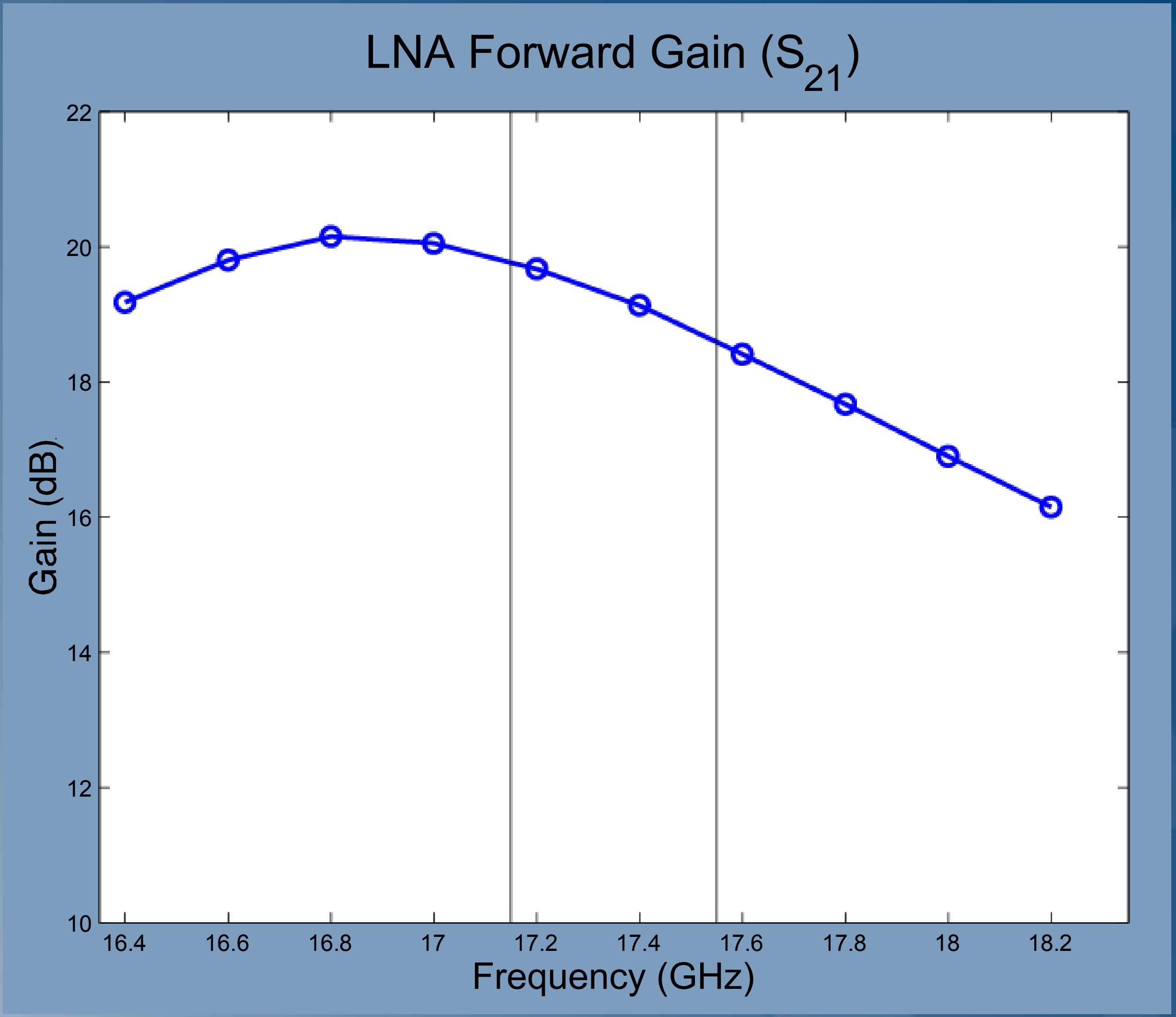
- Two-stage design to achieve high gain
- Both biased for low noise
- First stage noise/power matched to 50Ω
- Second stage not degenerated for higher gain

LNA Layout

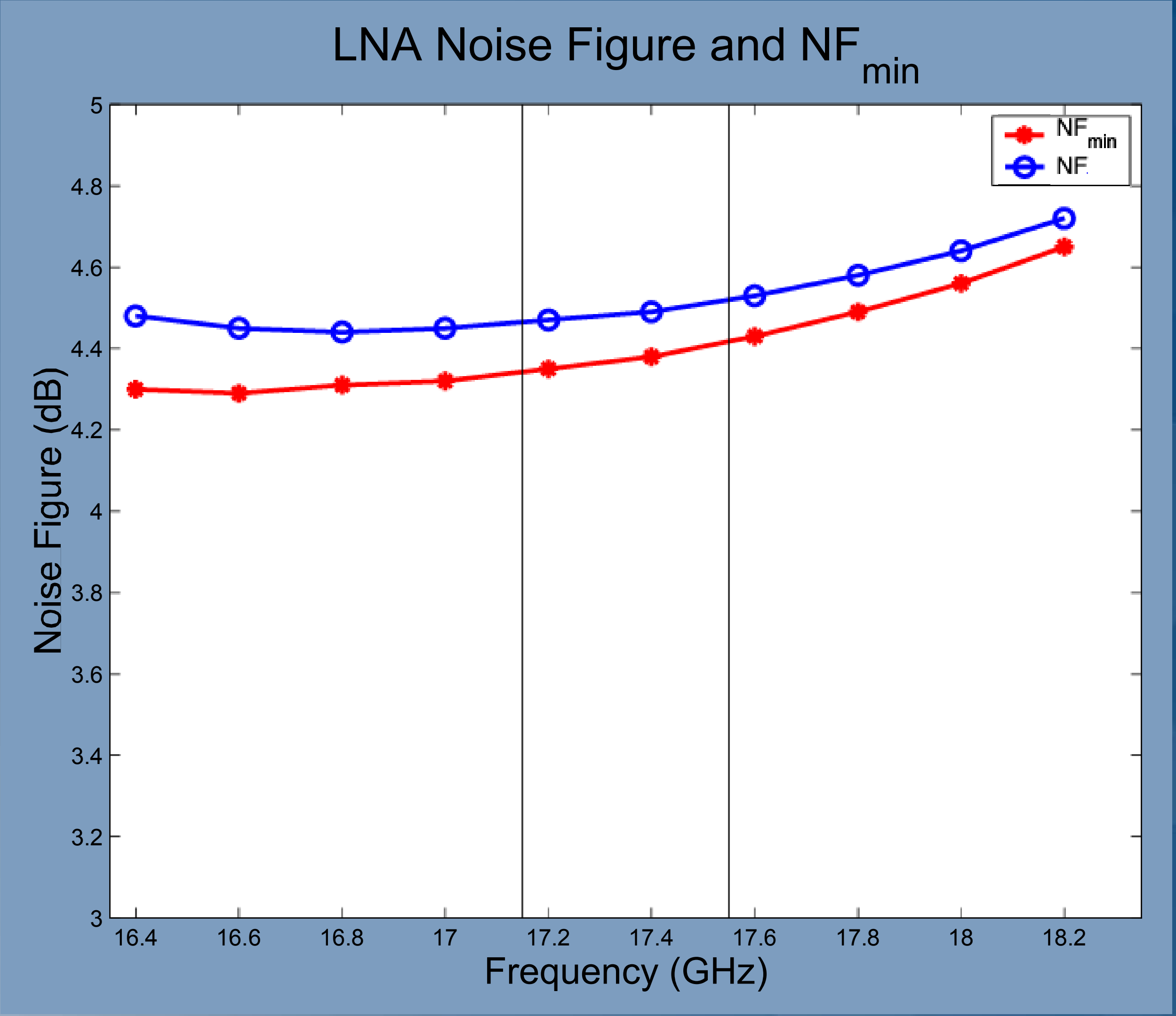
- IBM SiGe 5HP
  - f_T=50GHz
- 910µm x 1060µm
- picoHenry Inductors
- Simulated results based on extracted parasitics



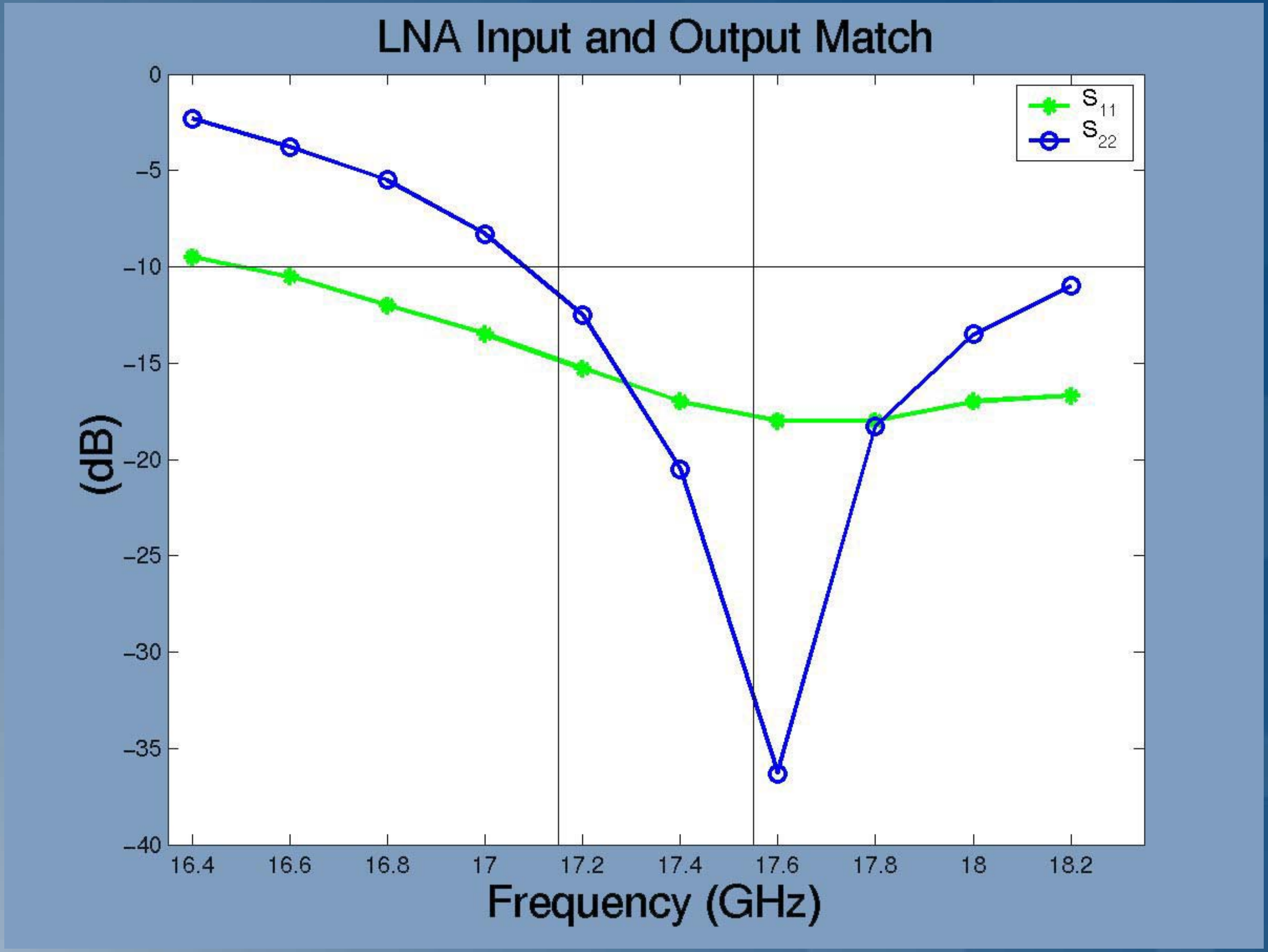
LNA Results : Gain = 19.5dB



LNA Results : NF = 4.5dB



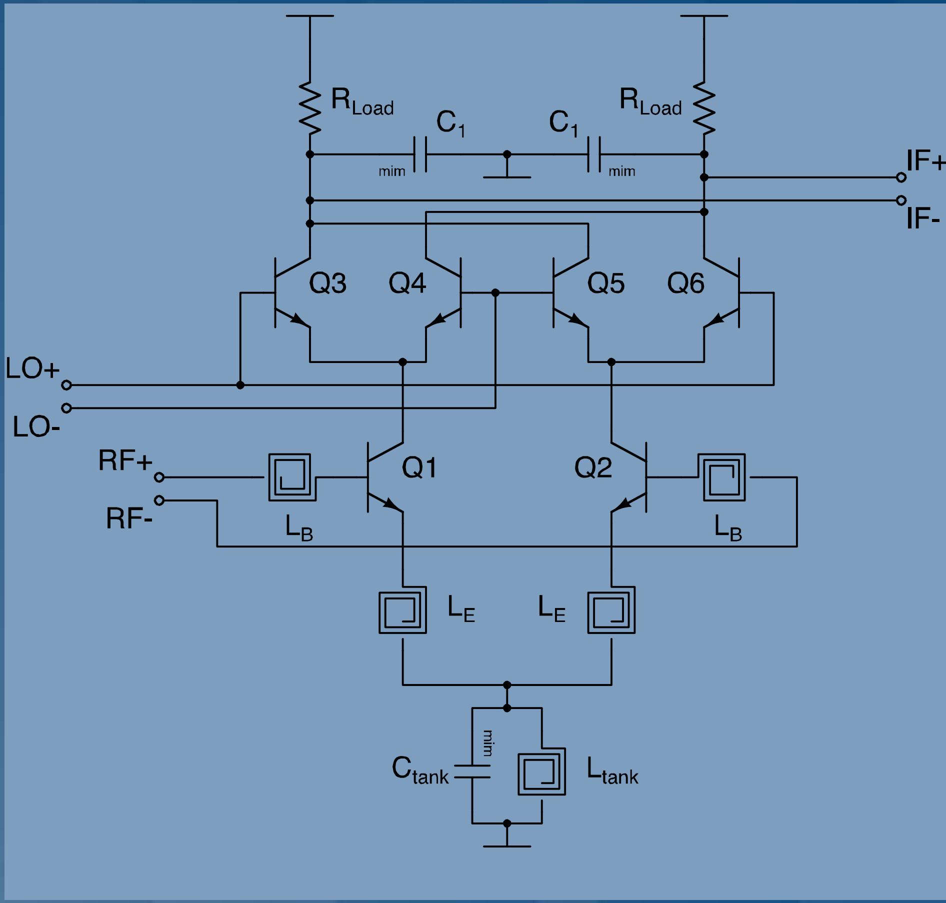
LNA Results : S_{11}, S_{22} < -10dB



Mixer Design and Results

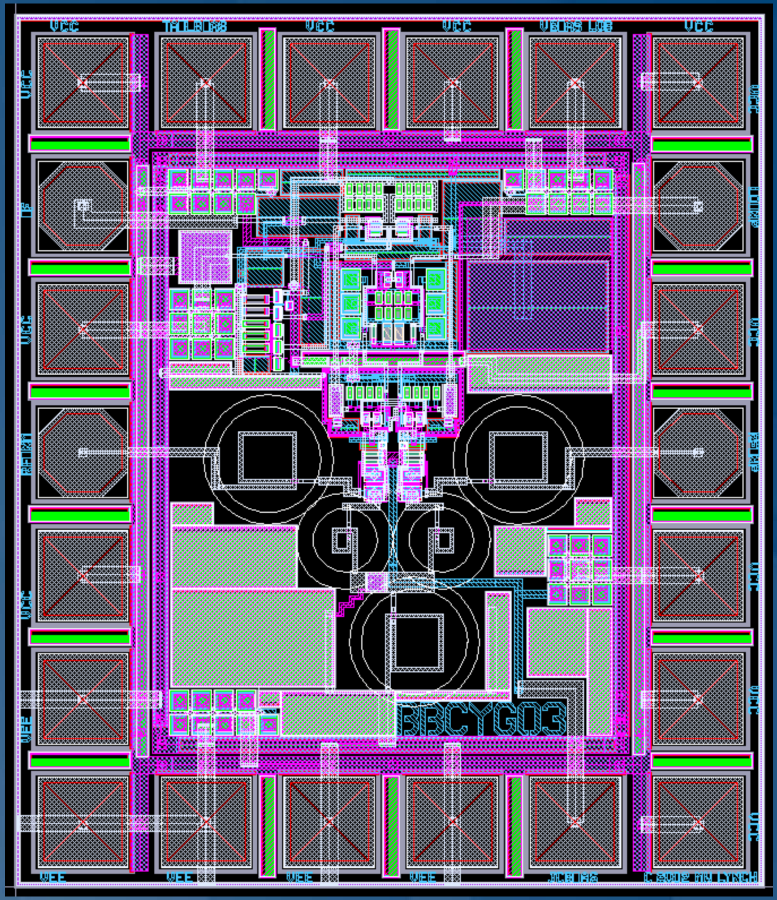
Mixer Schematic

- Noise/Power matching technique applied to Gm-pair (Q1-Q2)
- Mixing Quad (Q3-Q6) sized to maximize f_T
- Resistive loads for direct down-conversion
- Tail current source replaced with resonant tank

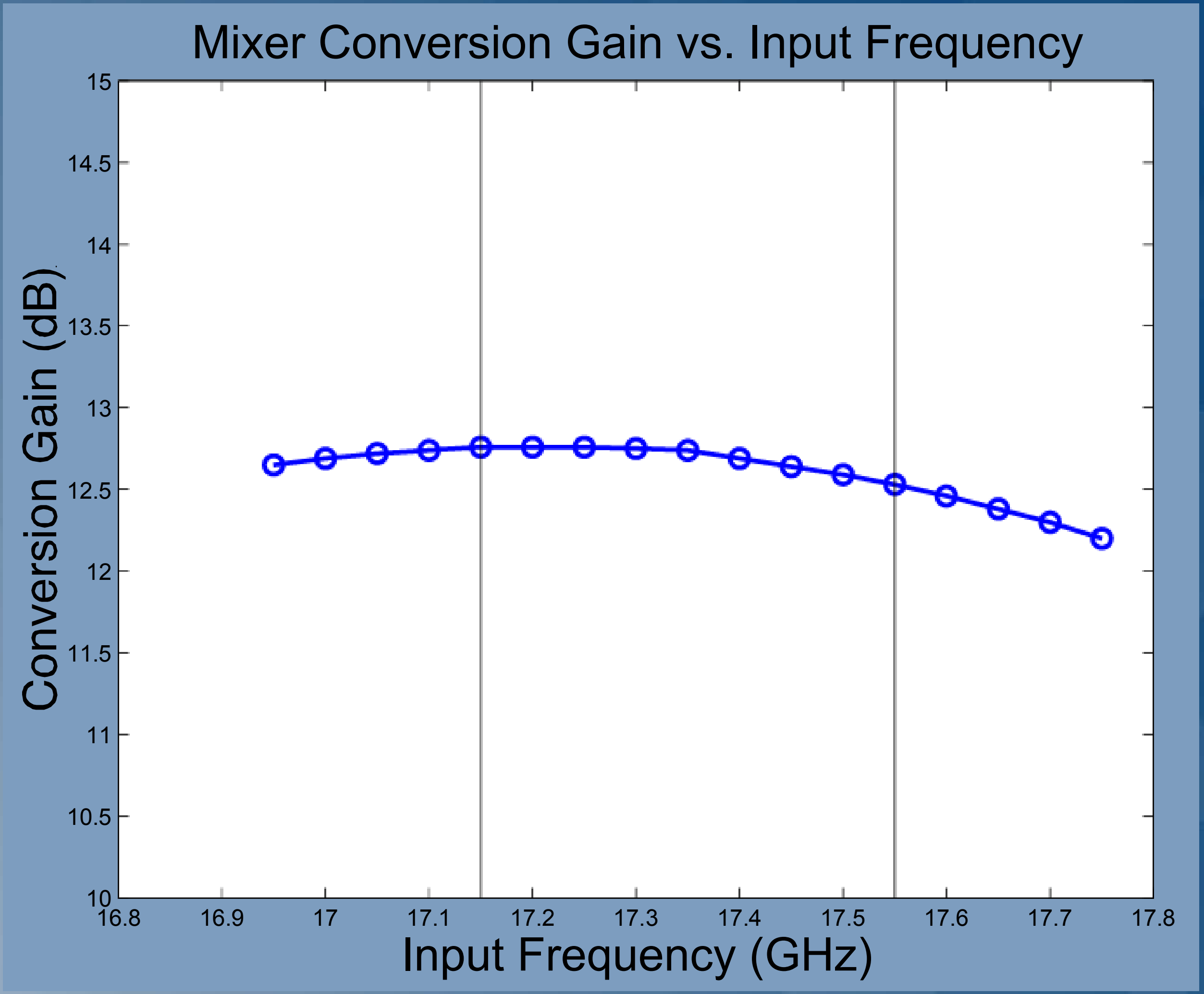


Mixer Layout

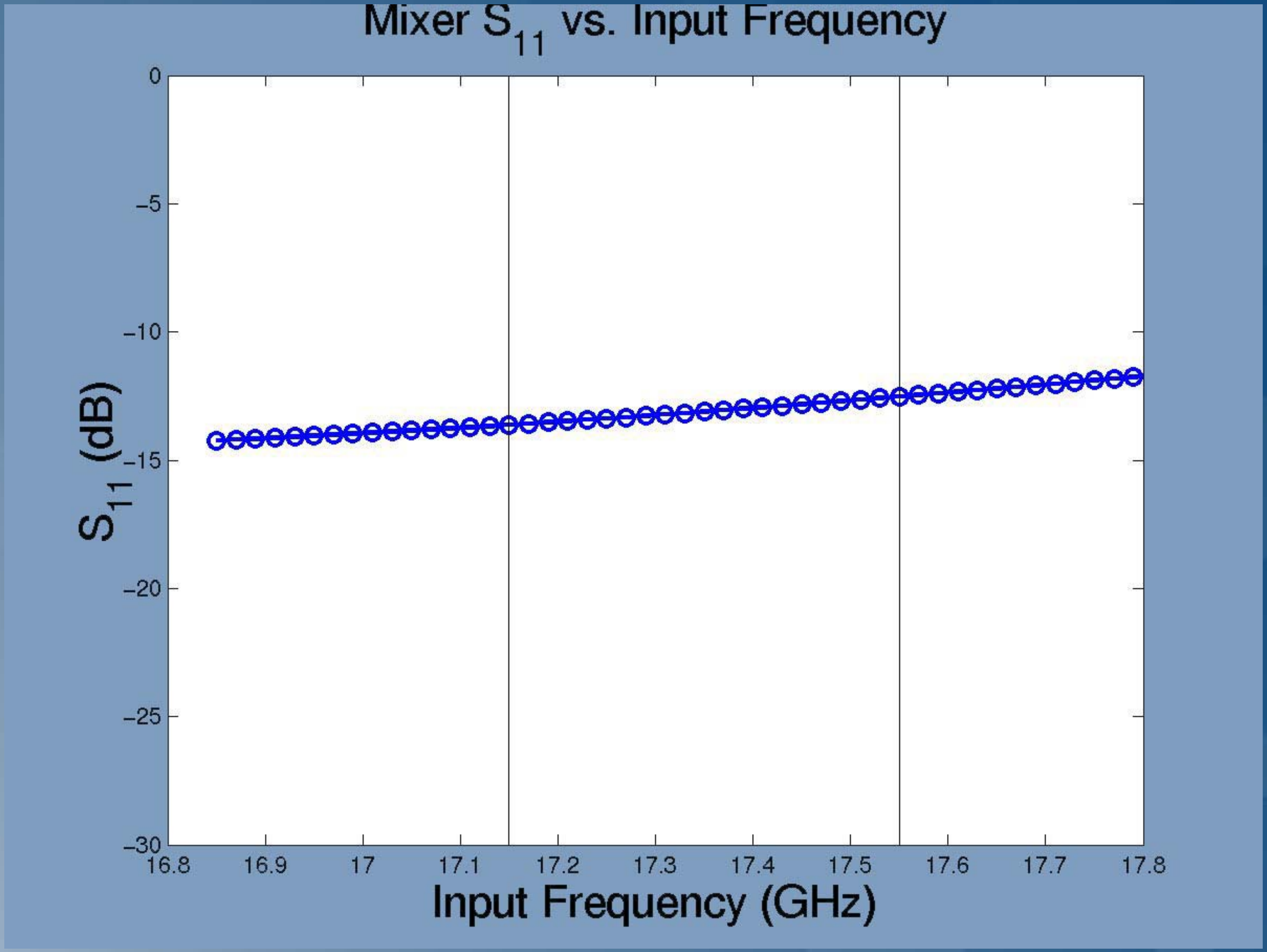
- IBM SiGe 5HP
- 910μm x 1060μm
- Active baluns
  - singled ended⇔double ended
  - LO & Baseband buffers
- Simulated results based on extracted parasitics



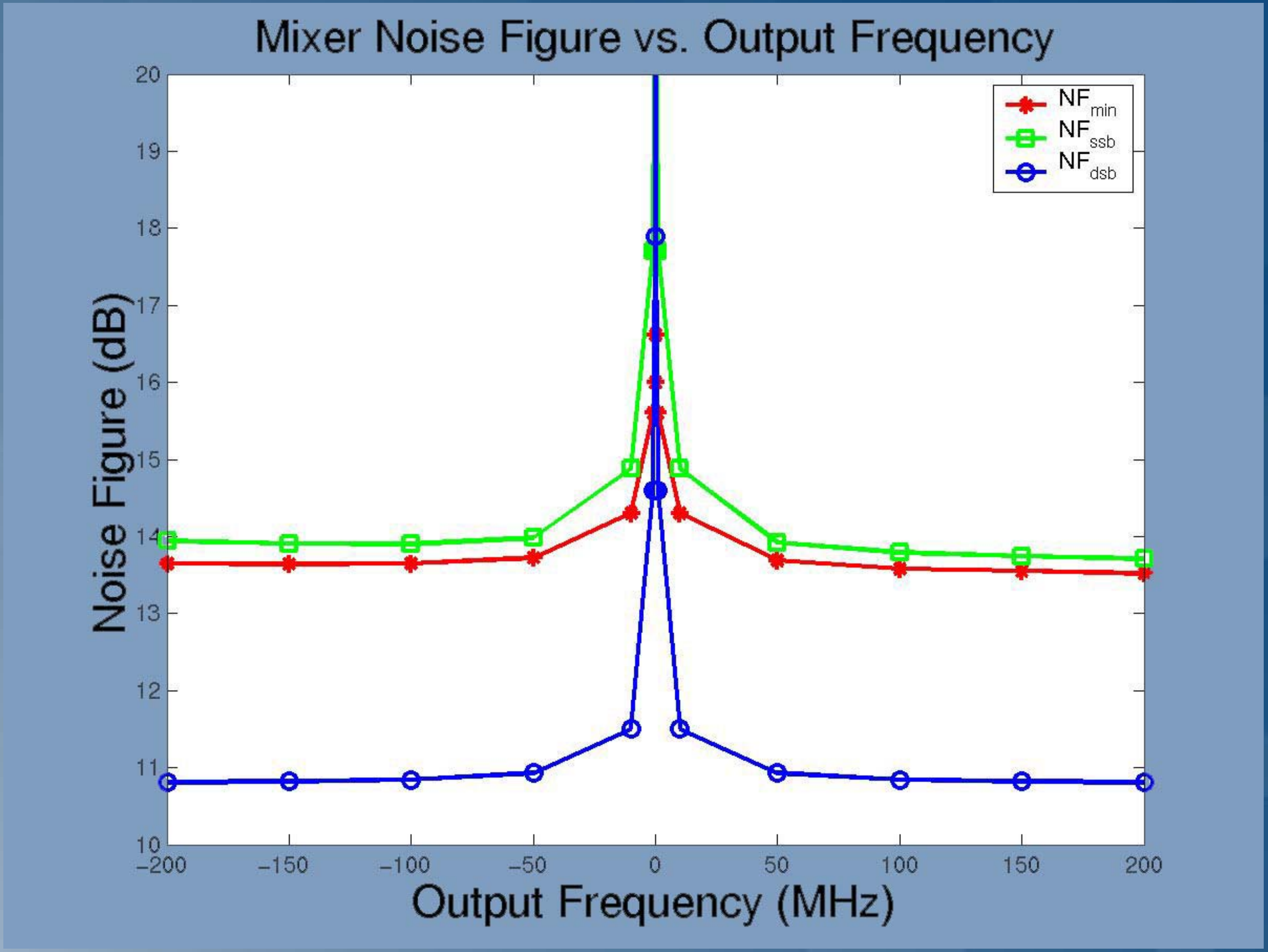
Mixer Results : Conv. Gain = 12.7dB



Mixer Results : S_{11} < -10dB



Mixer Results : NF_{DSB}=10.8dB



Summary and Future Work

- GigaRFIC project
  - Creating 17GHz WLAN RFICs
- Low Noise Biasing Technique
  - (J_{Copt}, I, L_E, L_B)
- 17.35GHz LNA and Direct Downconversion Mixer
- Fabricated devices expected in the last half of this year

Acknowledgements

- NSERC www.nserc.ca
- Alberta iCORE www.icore.ca
- TRLabs www.trlabs.ca
- Canadian Microelectronics Corporation www.cmc.ca

Questions

University of Calgary RFIC Research Group

www.atips.ca/groups/rfic