

©1997 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

This copyright notice is taken from the IEEE PSPB Operations Manual, section 8.1.10 entitled "Electronic Information Dissemination". At the time of this notice, this section is posted at

[http://www.ieee.org/portal/index.jsp?pageID=corp\\_level1&path=about/documentation/copyright&file=policies.xml&xsl=generic.xsl](http://www.ieee.org/portal/index.jsp?pageID=corp_level1&path=about/documentation/copyright&file=policies.xml&xsl=generic.xsl)



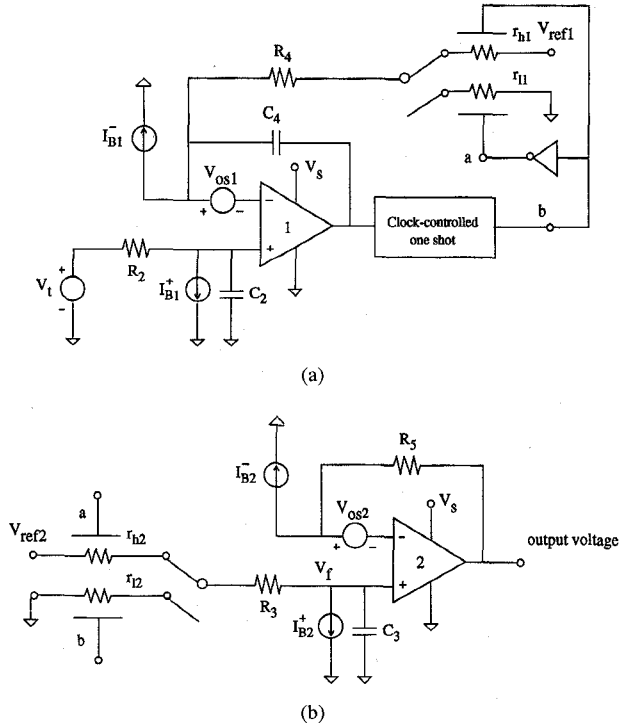


Fig. 2. Circuits for input bias current and input offset voltage analysis of the integrator and the lowpass filter. For single-ended operation, finite CMRR is taken into account by adding  $V_S/(2\text{CMRR})$  to  $V_{os1}$  and  $V_{os2}$ .

and the output frequency  $f$  will be given by

$$f = \frac{1}{N_1 T_c} \sqrt{\frac{V_t}{V_{\text{ref}2}}} \quad (5)$$

The effect of a finite  $R_3 C_3$  is considered in Section IV.

If a strain gauge bridge pressure transducer powered by  $V_{\text{ref}2}$  is used to measure the pressure drop, its output,  $V_t$ , will be proportional to  $V_{\text{ref}2}$  and  $V_{\text{ref}2}$  will cancel in (5) to produce a fully ratiometric measurement system with a long-term stability determined only by the stability of the clock producing  $T_c$  and the properties of the pressure transducer.

### III. ERROR ANALYSIS

The effects of mismatches in the "on" resistances of the switches S1 and of integrator operational amplifier bias currents, input offset voltage and common-mode rejection ratio must be considered in the above VFC. The effects of these nonidealities can be included in writing the charge balance for  $C_4$  [Fig. 2(a)] to give

$$\frac{M}{T} = \frac{\frac{V_t'}{V_{\text{ref}1}} + \frac{I_{B1}^-(R_4 + r_{h1})}{V_{\text{ref}1}}}{1 - \left(1 - \frac{V_t'}{V_{\text{ref}1}}\right) \frac{r_{h1} - r_{l1}}{R_4 + r_{l1}}} \quad (6)$$

where

$$V_t' = V_t + V_{OS1} + \frac{V_S - V_t}{\text{CMRR1}} - I_{B1}^+ R_2. \quad (7)$$

Similarly, the effect of mismatches in the "on" resistance of the switches that connect  $V_{\text{ref}2}$  and ground to the low pass

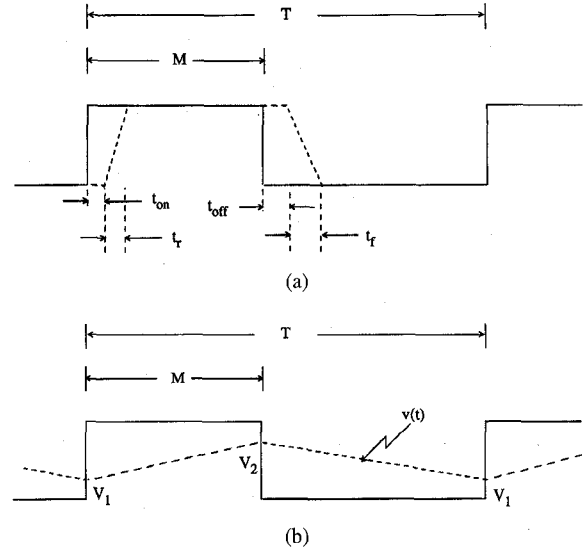


Fig. 3. (a) Analysis of the effect of pulse shape and delays on converter accuracy and (b) finite  $\tau = R_3 C_3$  on converter accuracy.

filter and the effects of bias currents and input offset voltage of the buffer amplifier can be assessed for a very long filter time constant by writing a charge balance for the filter capacitor [Fig. 2(b)] to give

$$\frac{V_f}{V_{\text{ref}2}} = \frac{\frac{M}{T} - \frac{I_{B2}^+(R_3 + r_{h2})}{V_{\text{ref}2}}}{1 + \left(1 - \frac{M}{T}\right) \frac{r_{h2} - r_{l2}}{R_3 + r_{l2}}} \quad (8)$$

and

$$\begin{aligned} V_{\text{ref}1} = V_{\text{oave}} = & \left(\frac{V_f}{V_{\text{ref}2}}\right) V_{\text{ref}2} + V_{OS2} \\ & + \frac{V_S}{2} - \frac{V_f}{V_{\text{ref}2}} V_{\text{ref}2} \\ & + \frac{V_S}{\text{CMRR2}} + R_5 I_{B2}^-. \end{aligned} \quad (9)$$

In (6)–(9), the subscripts 1 and 2 refer to amplifier number; CMRR is the common mode rejection ratio;  $I_B^-$  and  $I_B^+$  are the amplifier input bias currents for the inverting and noninverting terminals;  $r_{h1}$  and  $r_{l1}$  are switch resistances when  $R_4$  is connected to  $V_{\text{ref}1}$  and ground, respectively;  $r_{h2}$  and  $r_{l2}$  are switch resistances when  $R_3$  is connected to  $V_{\text{ref}2}$  and ground, respectively; and  $V_f$  is voltage across capacitor  $C_3$ .

Errors due to the sets of switches S1 and S2 and to imperfect lowpass filtering as indicated in Fig. 3 are given by the following expressions.

#### A. Error Due to Switches S1 and S2 [Fig. 3(a)]

The frequency error in percent of full-scale is given by

$$\text{FSE, \%} = \left[ \frac{M}{T} - \sqrt{\frac{V_t}{V_{\text{ref}2}}} \right] \times 100 \quad (10)$$

where

$$\frac{M}{T} = \sqrt{\frac{V_t}{V_{\text{ref}2}}} \cdot \frac{1}{1 + \frac{\Delta t}{N_1 T_c}} \quad (11)$$

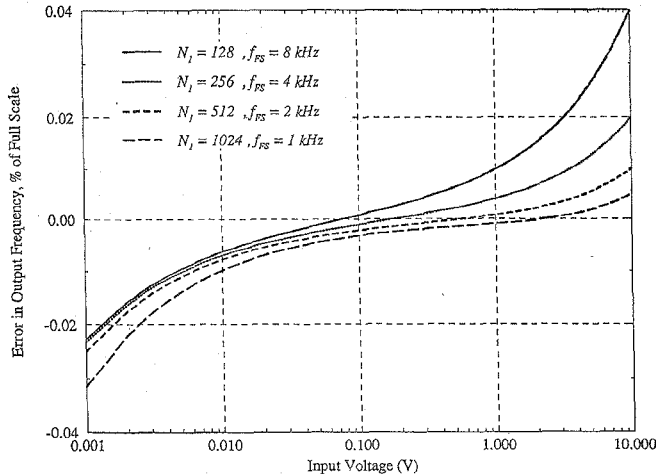


Fig. 4. Calculated total worst-case error.

### B. Error Due to Finite Lowpass Filter Time Constant $\tau = R_3 C_3$ [Fig. 3(b)]

The frequency error in percent of full-scale is given by

$$\text{FSE, \%} = \left[ \frac{M}{T} - \sqrt{\frac{V_t}{V_{\text{ref}2}}} \right] \times 100 \quad (12)$$

where

$$\frac{V_t}{V_{\text{ref}2}} = \frac{M}{T} \left[ 1 - \frac{\tau (1 - e^{-(T-M/\tau)})(1 - e^{-(M/\tau)})}{1 - e^{-(T/\tau)}} \right] \quad (13)$$

As an example, suppose auto-zeroing amplifiers such as the TS913A are used in a single-ended configuration with  $V_S = 15$  V.  $V_{OS}$  can be as high as  $15 \mu\text{V}$ , the CMRR can be as low as 110 dB, and the bias currents can be as high as 90 pA with a possible mismatch between  $I_B^+$  and  $I_B^-$  of 20 pA at  $25^\circ\text{C}$ . If 4066 CMOS analog switches are used,  $r_h - r_l$  can be as high as  $50 \Omega$ . If  $R_3 = 1 \text{ M}\Omega$ ,  $C_3 = 0.22 \mu\text{F}$ , and  $\Delta t = -50 \text{ nS}$ , a reasonable value for the 4066 switches, the total error in the output frequency calculated using (6)–(13) is given in Fig. 4. It appears that 0.02% of full-scale accuracy is possible at low oscillator frequencies and large  $R_3 C_3$ .

## IV. EXPERIMENTAL RESULTS AND CONCLUSIONS

Results of measurements on the circuit of Fig. 1 are presented in Fig. 5. The clock frequency,  $f_c$ , in each case was 1.024 MHz with  $N_1 = 1024$ ,  $N_1 = 512$ ,  $N_1 = 256$ , and  $N_1 = 128$  yielding full-scale frequencies,  $f_{FS}$ , of 1, 2, 4, and 8 kHz, respectively. No adjustments other than the setting of  $f_c$  were required to achieve 0.02% of full-scale accuracy in the input voltage range from 1 mV to 10 V for full-scale frequencies of 1, 2, and 4 kHz. At a full-scale of 8 kHz, the error at higher input voltages begins to increase to a more substantial level. The calculated error curve shown in Fig. 4 is in good agreement in both shape and magnitude with that which was measured. It can be shown that the errors for  $(V_t/V_{\text{ref}2}) \rightarrow 1$  are due primarily to pulse-shape-related effects, whereas the errors for  $(V_t/V_{\text{ref}2}) \rightarrow 0$  are due primarily to amplifier offset voltages, amplifier finite common-

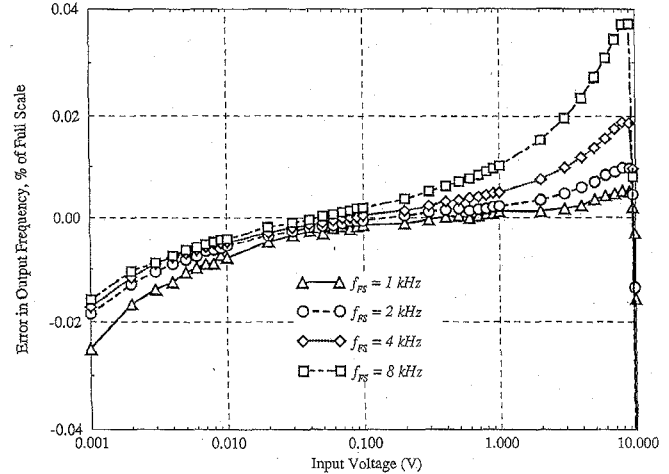


Fig. 5. Measured errors. Error in percent of full-scale =  $100 \times [f_{\text{meas}} - f_{FS} \sqrt{V_t/V_{\text{ref}2}}] / f_{FS}$ .

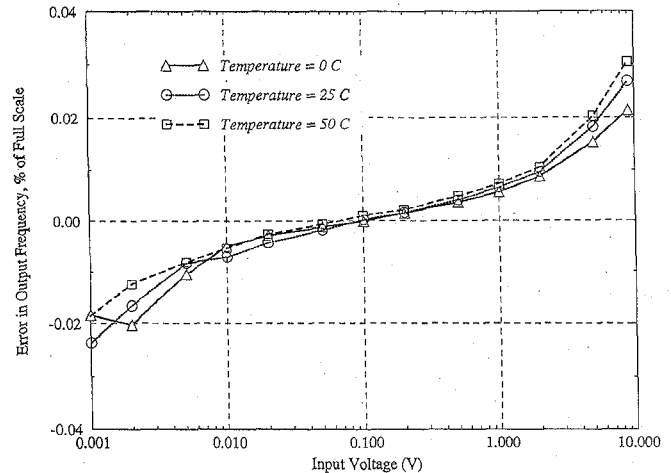


Fig. 6. Measured errors as a function of temperature. Error in percent of full-scale =  $100 \times [f_{\text{meas}} - f_{FS} \sqrt{V_t/V_{\text{ref}2}}] / f_{FS}$ .

mode rejection ratios, and to ripple on  $V_{\text{ref}1} = V_{\text{Oave}}$ . The ripple component of the error cannot, of course, be reduced without increasing the system response time to changes in  $V_t$ .

As noted earlier, and as is evident from (5), the voltage-to-frequency transfer function is independent to first order of passive component values. Since the operational amplifiers are auto-zeroed, this transfer function should be practically independent of temperature if  $V_{\text{ref}2}$  and  $T_c$  are fixed. Error plots for  $f_{FS} = 4$  kHz operation at 0, 25, and  $50^\circ\text{C}$  are shown in Fig. 6 to confirm this property of the converter. In generating Fig. 6, the amplifiers and switches were changed from those used to generate Fig. 5 to show that there is practically no sensitivity to those components as well.

In conclusion, the clock-controlled square-rooting VFC is capable of 0.02% of full-scale accuracy operation when constructed with commercially-available 18 V CMOS components and 18 V auto-zeroed amplifiers. If a crystal-controlled VFC is used as part of a flow measuring system where a strain gauge bridge pressure transducer is operated ratiometrically, the above level of performance can be expected from the signal processing circuits.

## REFERENCES

- [1] F. N. Trofimenkoff, C. O. Li, and D. J. Paslawski, "Clock-controlled voltage-to-frequency converter," U.S. Patent 4847620, July 11, 1989; Canadian Patent 1288165, Aug. 1991.



**F. N. Trofimenkoff** (M'63-SM'69) was born in Veregin, Sask., Canada, on August 10, 1934. He received the B.E. degree in engineering physics and the M.Sc. degree in physics, both from the University of Saskatchewan, Saskatoon, in 1957 and 1959, respectively. He was awarded an Athlone Fellowship in 1959 and received the Ph.D. degree in electrical engineering (semiconductor device physics) from the University of London, Imperial College of Science and Technology, London, U.K., in 1962.

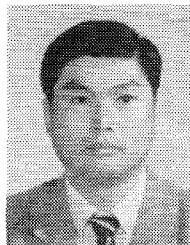
From 1957 to 1959, he worked on instrumentation for accurate humidity measurement in the Division of Building Research, National Research Council of Canada, and from 1962 to 1966 he was an Assistant Professor of Electrical Engineering at the University of Saskatchewan. In 1966, he joined the Electrical Engineering Department, University of Calgary, Calgary, Alta., Canada. His current research interests are in the circuits and devices area and in instrumentation related to the petroleum industry.

Dr. Trofimenkoff is a member of the Association of Professional Engineers, Geologists and Geophysicists of Alberta, the Engineering Institute of Canada, the Canadian Association of Physicists, and the American Society for Engineering Education.



**Farmarz Sabouri** (M'95) was born in Tehran, Iran, in 1965. He received the B.Sc. degree in electrical engineering in 1987 from Ferdowsi University, Mashad, Iran, the M.Sc. degree in electrical engineering in 1990 from the Sharif University of Technology, Tehran, and the Ph.D. degree in electrical engineering from the University of Calgary, Calgary, Alta., Canada, in 1996.

From 1990 to 1992, he was a Part-Time Instructor at Ferdowsi University, and a Research Engineer at the Sajad Electrical Research Center and the Trakho Ballast Manufacturing Co., Mashad. He is currently with Analog Devices, Somerset, NJ, where he designs high-speed analog-to-digital converters. His current research interests include high-speed data converters and switched capacitor circuits.



**Jichang Qin** was born in Beijing, China, in 1951. He received the B.S. and M.S. degrees from the Beijing Institute of Chemical Technology in 1982 and 1984, respectively. In 1988, he received the M.S. degree in electrical and computer engineering from the University of Calgary, Calgary, Alta., Canada, in 1991.

He was a Lecturer at the Beijing Institute of Chemical Technology from 1985 to 1988 and worked on the development of semiconductor pressure transducers. He has worked in the oil and gas industry and is currently an Electronics Designer with McAllister Petroleum Services Ltd., Calgary.



**J. W. Haslett** (M'64-SM'79) was born in Saskatchewan, Canada, on September 27, 1944. He received the B.Sc. degree in electrical engineering from the University of Saskatchewan, Saskatoon, Sask., Canada, in 1966 and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Calgary, Calgary, Alta., Canada, in 1968 and 1970, respectively.

In 1970, he joined the Department of Electrical Engineering, University of Calgary, and served as Head from 1986 to 1997. His current research interests include optical imaging systems for spacecraft applications, instrumentation systems related to drill stem testing of oil and gas wells, high-temperature semiconductor device behavior, and the design of analog and digital VLSI circuits.

Dr. Haslett is a member of the Association of Professional Engineers, Geologists and Geophysicists of Alberta, the Canadian Astronomical Society, the Canadian Society of Exploration Geophysicists, and the American Society of Engineering Education.