A 1.5V 12mW Silicon Receiver Front-end with a 65dB Image Rejection

University of Calgary
RFIC Research Group

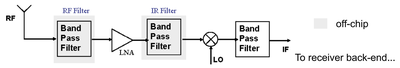
MISSION STATEMENT: The semiconductor Indusry Association (SIA) predicts that 50% of new design in the next two years will be based on previously implemented designs. Compaines worldwide are gearing up for this change and making organizational adjustments to rapidly adopt design reuse methodolgies. They are leveraging reuse to handle SOC complexity. *Mentor Graphics* develops simulation environment enabling wireless IP and design reuse. This environment dramatically reduces the design cycle , resulting in a substantial reduction in time to market. **our mission is** to provide a high-performance, proven IP blocks to SOC used in the wireless communication market. These IP elements, when combined with a suitable microcontroller core, permit the implementation of a single chip GSM solution using industry standard CMOS process technologies.

Research Objective

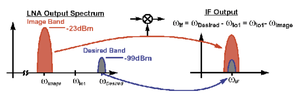
Lowering of complexity, power dissipation, and the number of external components in the front-end receiver used in most of the commercially available mobile receivers, a superheterodyne receiver. The designed system will be used in Mentor Graphics project: Technology Migration for RF systems as wireless IP block.

1. Motivation and Challenges

- **Superheterodyne Architecture is the most widely accepted for robust operation.** (Superior *selectivity* and *sensitivity*)

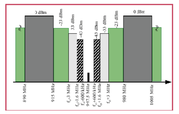


- **Image signal filtering is mandatory in this receiver !**



The image frequency problem is significant because while wireless standards restrict the output power of their own users, they have no control over adjacent bands.

- **High Q bandpass filter is required to achieve the required IR in cellular standards.**



Blocking Signals Levels for GSM Standard

$IR_{required} = -80dBm - (-23dBm) + SNR_{required}$

$IR_{required} = 65$ dB with IF=325-MHz

- **On-chip BP filter with 65dB IR in GHz range is *extremely* challenging due to LOW Q of CMOS inductors (<10).**

- Currently, most of the *commercially* available mobile receivers use off-chip passive BP filters such as **ceramic** or **SAW** filters.

- Exploring new on-chip IR **circuit techniques** adapting the low Q CMOS inductor is required to permit SOC integration solution.

- In principle IR Architectures could be implemented on-chip but they have a limited IR value due to the process constraint.

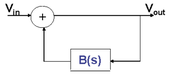
2. Proposed IR Technique

A *notch filter* centered at the image frequency to eliminate it.

(1) Theory of operation:

$$B(s) = \frac{G_{BP} \cdot (\omega_0/Q) \cdot s}{s^2 + s \cdot (\omega_0/Q) + \omega_0^2}$$

$$H(s) = \frac{s^2 + s \cdot (\omega_0/Q) + \omega_0^2}{s^2 + s \cdot (\omega_0/Q) \cdot (1 + G_{BP}) + \omega_0^2}$$



Closed-loop transfer function : $H(s) = (V_{out}/V_{in})$

Second-order bandpass Transfer function : B(s)

- The expression exhibits a pair of complex zeros. Theses zeros create a notch in the frequency response and thus a **notch filter** has been obtained.
- This shows that it is sufficient to inserte a **BP response** in the feedback loop to synthesize a pair of complex zeros in the closed-loop response.

$$H(s) = \frac{1}{(1 + G_{BP})} : \text{ at } \omega = \omega_0$$

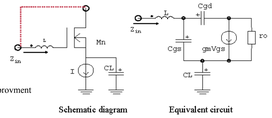
- The Q term does not appear : Low Q BP filter = notch with very high Q, provided the BP filter has large gain.

(2) Implementation:

To implement the block diagram shown above a feed-back element (*A*) and a summer node (*B*) are needed.

A. 2nd order BP Active Filter B(s):

Consider the series resonator shown in Figure. It cosists of an on-chip inductor in series with C-degenrate NMOS transistor It is biased by means of the ideal current source I.



$$Y_{in} = \frac{s.C_s\left(1 + \frac{g_m}{s.C_{gs}}\right)}{s^2.L.C_s + s.C_s.\left(R + \frac{g_m}{s^2.C_{gs}.C_L}\right) + 1}$$

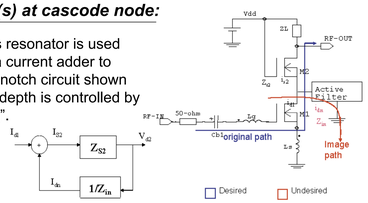
IR improvment

Pair of complex poles — losses — negative term

Y_{in} can be used as the feedback element in a current summing block diagram...

B. Active filter B(s) at cascode node:

The enhanced series resonator is used in combination with a current adder to obtain the cascoded notch circuit shown in Figure. The notch depth is controlled by adjusting I, "Q tuning".



- The notch Filter transfer fuction is:

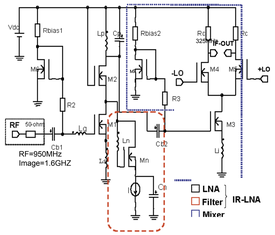
$$\frac{I_{s2}}{I_{d1}} = \frac{\overbrace{-\omega^2.L_n.C_{gsn} + j\omega.C_{gsn}.\left(R - \frac{g_m}{\omega^2.C_{gsn}.C_n}\right) + 1}^{\text{Zeros (notch)}}}{-\omega^2.L_n.C_{gsn} + j\omega.C_{gsn}.\left(R - \frac{g_m}{\omega^2.C_{gsn}.C_n}\right) + Z_{s2}.j\omega.C_{gsn}.\left(1 + \frac{g_m}{j\omega.C_{gsn}}\right) + 1}$$

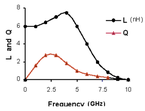
Notch depth

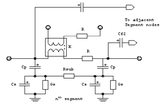
- *This principle has been used to modify the transfer function of a cas code LNA circuit (IR-LNA).*

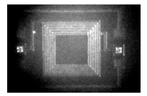
3. Silicon Receiver Front-end

The complete schematic of the image reject front-end receiver consisting of a capacitive coupled IR-LNA and a mixer is shown in the right Figure. It has been designed in a **standard CMOS technology.** The design is dedicated to be used in .18μ CMOS technology. It is designed to operate at an RF of 950-MHz for 325-MHz IF. The image signal is located at 1.6-GHz. It consumes 11.7 mW of power from 1.5-V supply. The receiver uses three square spiral inductors L_p, L_n, and L_l, and one bondwire inductor L_s. The spirals are fabricated in metal-three and surrounded by a guard ring to minimize the interaction between them. The die photo, L&Q plots and the model are shown below.





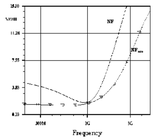


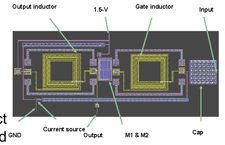


Inductance	6-nH
Q @ 950-MHz	1.8
Q @ 1.6-GHz	2.5
Resonance Freq.	9-GHz

1. Low Noise Amplifier

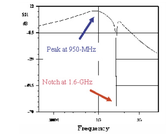
The LNA topology is derived from an *RF tuned amplifier* to achieve high selectivity (6dB) and to minimize the power. The device width of M_1 is chosen to achieve the minimum noise figure at 950 MHz as shown in the right Figure. It has a NF of 1.8dB and consumes 7.1mW of power. At 950 MHz, the LNA core has a power gain S_{21} of 13dB with 50Ω output termination. A 1.3-nH bondwire inductor is used to produce 50 Ω at the input which needed to terminate the transmission line. The LNA layout is shown in the right Figure.



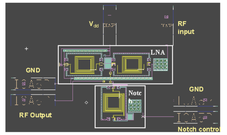


2. Image-Reject LNA

The filter is incorporated into the LNA core to reject the image signal. The circuit has been achieved a maximum image rejection of 65 dB at 1.6 GHz without requiring a high Q inductor. Also, the gain is still boosted at 950 MHz as shown in the right Figure. The bandwidth of the image reject notch is 20 MHz. The IR-LNA NF is 2.4dB and consumes 10.3mW of power. This table shows the image rejection values with the percentage of variation in the value of I_{max}. In a more relaxed design, it is possible to decrease the amount of rejection by decreasing the power consumption of the filter.



$\Delta I_{max}/I_{max}$	0	0.1%	0.5%	1%	2%	5%
IR	65dB	57dB	40dB	34dB	27dB	22dB



3. Gilbert cell mixer

The output of the IR-LNA is downconverted by a single balanced mixer to produce the 325 MHz IF signal . The mixer core transistor is biased near threshold voltage to operate at a 1.5V supply. 0 dBm of LO power is driven into each side of the mixing core. The two input signals located at 800 kHz away from each other are applied to the mixer RF port to measure the linearity. The IIP3 is –7 dBm.

4. Front-end Receiver

The whole front-end has an overall sensitivity of -80dBm when a minimum SNR of 9 dB is achieved at the output. The performance for the receiver front-end has a 32dB conversion gain, 5.4dB noise figure, -24dBm input IP3, and 61dB of image rejection. The total power consumption at 1.5 V supply is 11.7mW. Comparing with previous work is shown below, all these works designed using the same CMOS Technology.

IR- Tech. based	RF/IF	IR	IP3	NF	Power
Hartley	900/70 MHz	44dB	-4.7dBm	9.3	21 mW
Weaver	900/400MHz	40dB	-8 dBm	4.7	72 mW
Weaver	900/3 MHz	46dB	-27 dBm	24	500mW
Notch	900/325MHz	61dB	-24 dBm	5.4	12 mW

Summary

Using on-chip inductors, a 950 MHz silicon monolithic superheterodyne receiver front-end suitable for portable radio applications has been demonstrated. The receiver integrates an LNA with an image rejection notch filter and a Gilbert cell mixer. The results show that the notch filter technique works well for image rejection, and a very high Q can be obtained.The receiver front-end performance has a 5.4dB NF, -24dBm input IP3, and 61dB of IR. The total power consumption at 1.5 V supply is 11.7mW. Providing on-chip IR solution permits wireless IP design reuse and technolohy migration.

University of Calgary ELECTRICAL & COMPUTER ENGINEERING
TRLabs
NSERC CRSNG
Mentor Graphics

A. Youssef, W. Badawy, J. Haslett